Francesco Conti

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Employment History

September 2022 – current
Senior Assistant Professor (RTD-B), University of Bologna, Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (DEI).

May 2020 – current (intermittent)
External consultant, GreenWaves Technologies.

June 2020 – September 2022
Junior Assistant Professor (RTD-A), University of Bologna, Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (DEI).

June 2016 – June 2020
Postdoctoral Researcher, ETH Zürich, Integrated Systems Laboratory, Department of Information Technology and Electrical Engineering (D-ITET).

Research Grant Holder, University of Bologna, Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (DEI).

January 2013 – June 2016
Doctoral Student, University of Bologna, Department of Electrical, Electronic, and Information Engineering "Guglielmo Marconi" (DEI). PhD in "Ingegneria Elettronica, delle Telecomunicazioni e Tecnologie dell'Informazione", XXVIII cycle.

Education

2013 – 2016
Ph.D., University of Bologna in Ingegneria Elettronica, delle Telecomunicazioni e Tecnologie dell'Informazione.
Thesis title: *Heterogeneous Architectures for Parallel Acceleration.*

2010 – 2012
M.Sc. University of Bologna in Ingegneria Elettronica (110/110 with honours).
Thesis title: *Design an Implementation of a Heterogeneous Multicore Shared Memory Cluster for Embedded Computer Vision Applications on FPGA and SoC Platforms.*

2008 – 2010
B.Sc. University of Bologna in Ingegneria Elettronica (110/110 with honours). Thesis title: *Progettazione ed ottimizzazione di readout digitale veloce di sensori a matrice di pixel per la prossima generazione di esperimenti in fisica delle alte energie.*

Teaching Activity

Curricular Teaching Activities at the University of Bologna

2022/23 – current
35364 - Architetture Digitali per l'Elaborazione del Segnale M, module 1 (3 CFU) for the master degree in Electronic Engineering. Topics: evaluation metrics for digital signal processing architectures, architectural optimization techniques (pipelining, parallelism, multiplexing), design of digital systems for low-power digital signal processing.

2021/22 – current
93398 - Architectures for Artificial Intelligence M, module 2 (3 CFU) for the master degree in Electronic Engineering. Topics: computational characteristics of Deep Neural Networks (DNNs), DNN quantization, DNN acceleration on large platforms (GPUs) and tiny platforms (microcontrollers), design of advanced hardware accelerators for DNNs.

Teaching Activity (continued)

- **87198 - Statistics and Architectures for Big Data Processing M,** module 2 (3 CFU) for the master degree in Electronic Engineering; also available as *97467 - Big Data Analytics for Automotive Manufacturing Applications* for the master degree in Advanced Automotive Engineering. Topics: computer architecture, parallel computing, and heterogeneous acceleration techniques.

2022/23 – 2023/24
- **35364 - Architetture Digitali per l'Elaborazione del Segnale M,** module 1 (3 CFU) for the master degree in Electronic Engineering. Topics: evaluation metrics for digital signal processing architectures, architectural optimization techniques (pipelining, parallelism, multiplexing), design of digital systems for low-power digital signal processing.

2020/21
- **91259 - Architecture and Platforms for Artificial Intelligence,** module 3 (1.5 CFU) for the master degree in Artificial Intelligence. Topics: computational characteristics of Deep Neural Networks (DNNs), DNN quantization, DNN acceleration on large platforms (GPUs) and tiny platforms (microcontrollers).
- **86464 - Algorithms and Systems for Big Data Processing,** module 2 (3 CFU) for the master degree in Advanced Automotive Engineering. Topics: computer architecture, parallel computing, and heterogeneous acceleration techniques.

2018/19 – 2019/20
- **28651 - Elettronica T-A,** official course tutor for the bachelor degree in Ingegneria Gestionale, course lecturer Prof. A. Bartolini. Topics: basic digital circuits course.

Extra-curricular teaching activities

June 2024
- **Customizing RISC-V Based Microcontrollers,** 18 hours, ETH Future Computing Lab Summer School, Zurich, Switzerland.

September 2023
- **Elements of Machine Learning for Sensor and Edge Computing,** 4 hours, short Ph.D. course for Electronics, Telecommunications, and Information Technology Ph.D. degree, University of Bologna.

July 2022
- **RISC-V: Open ISA, Processors and Systems from AI-enabled IoT to HPC,** 6.25 hours, HiPeAC ACACES Summer School, Fiuggi, Italy.

July 2019
- **Machine Learning Accelerators: from Cloud to Edge,** 3 hours, ACM Summer School, Barcelona, Spain.

Supplementary Teaching Activity & Student Service

Supervision of Ph.D. Students

Cycle XXXIX
- **Alessandro Nadalini,** Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.

Cycle XXXVIII
- **Luka Macan,** Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
- **Luca Bompani,** Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.

Cycle XXXVII
- **Yvan Tortorella,** Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
- **Mahyar Pourjabar,** Ph.D. degree in Data Science and Computation, University of Bologna, University of Bologna.

Co-Supervision of Ph.D. Students

ongoing
- **Philip Wiese,** Doctor of Science at ETH Zürich.

Supplementary Teaching Activity & Student Service (continued)

- **Victor Jung,** Doctor of Science at ETH Zürich.
- **Gamze Islamoglu,** Doctor of Science at ETH Zürich.
- **Arpan Prasad,** Doctor of Science at ETH Zürich.

2024

- **Georg Rutishauser,** Doctor of Science at ETH Zürich.
- **Gianna Paulin,** Doctor of Science at ETH Zürich.

Cycle XXXIX

- **Riccardo Tedeschi,** Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.

Cycle XXXVII

- **Davide Nadalini,** Italian National Ph.D. degree in Artificial Intelligence, Politecnico di Torino.
- **Alberto Dequino,** Italian National Ph.D. degree in Artificial Intelligence, Politecnico di Torino.

Supervision of Master Theses

July 2024

- **Andrea Belano,** Computer Engineering. Thesis title: *Softex: Softmax Computing Engine for Fast Exponential Acceleration*.

March 2024

- **Luca Angeli,** Electronic Engineering. Thesis title: *Progetto di hardware per la conversione di protocolli applicato a sensori di immagini basati su eventi*.
- **Stefano Di Labio,** Electronic Engineering. Thesis title: *A Survey of Techniques and Architectures for Extended Reality Computing*.
- **Luigi Ghionda,** Electronic Engineering. Thesis title: *Design of a Multi-Precision Floating-Point FFT Hardware Accelerator*.
- **Athar Zafeer Kannamangalam Aslam Basha,** Electronic Engineering. Thesis title: *Automatic insertion of fault-injectable flip-flops in FPGA emulators of computing platforms*.

February 2024

- **Aurora Di Giampietro,** Electronic Engineering. Thesis title: *Integrating a Tensor Datapath into a Small and Efficient Vector Processor*.

March 2023

- **Michele Gaspari,** Computer Science. Thesis title: *Multi Source Speech Enhancement for Low-Power Micro-Controller devices*.

October 2022

- **Luca Bompani,** Artificial Intelligence. Thesis title: *Embedding Video Object Detection Capabilities on Low-Power Nano-Drones*.
- **Mattia Orlandi,** Artificial Intelligence. Thesis title: *Motor Unit Spike Trains Reconstruction from sEMG Signals for Gesture Classification on a Low-Power Processing Platform*.
- **Angely Jazmín Oyola Suarez,** Artificial Intelligence. Thesis title: *An Embedded In-Cabin Lightweight High-Performance 3D Gaze Estimation System*.

July 2022

- **Pierangelo Maria Rapa,** Electronic Engineering. Thesis title: *Design of a wearable platform for PPG analysis with multicore low-power processor*.

October 2021

- **Pietro Maltoni,** Electronic Engineering. Thesis title: *Progetto di un acceleratore hardware per layer di convoluzioni depthwise in applicazioni di Deep Neural Network*.
- **Hossein Shirali,** Electronic Engineering. Thesis title: *Semi-Automatic Image Labeling Method Based On Point Clouds*.
- **Yvan Tortorella,** Electronic Engineering. Thesis title: *Design of a Low-Precision Floating-Point Matrix Multiplication Accelerator for On-Chip Deep Learning*.

July 2021

- **Manuel Cintura,** Advanced Automotive Electronic Engineering. Thesis title: *An Embedded Data Logger for In-Vehicle Testing*.

Supplementary Teaching Activity & Student Service (continued)

- **Riccardo Gandolfi,** Electronic Engineering. Thesis title: *Design of a memory-to-memory tensor reshuffle unit for ultra-low-power deep learning accelerators*.
- **Mahyar Pourjabar,** Electronic Engineering. Thesis title: *Federated Continual Learning for Distributed Deep-Edge Devices*.

March 2021 — **Davide Nadalini,** Electronic Engineering. Thesis title: *Mixed Precision Online Learning on a Parallel Ultra-Low Power Platform*.

Co-Supervision of Master Theses

March 2024 — **Lorenzo Greco,** Electronic Engineering. Thesis title: *Progettazione di un cluster eterogeneo con acceleratore analogico per intelligenza artificiale basato su ePCM*.

October 2021 — **Alessandro Nadalini,** Electronic Engineering. Thesis title: *Progettazione ed ottimizzazione di un processore dedicato per accelerazione di reti neurali quantizzate a precisione mista*.

July 2021 — **Mattia Sinigaglia,** Computer Engineering. Thesis title: *Progettazione ed implementazione di un Sistema On Chip per applicazioni audio*.

Supervision of Bachelor Theses

July 2024 — **Antonio D'Alessandro,** Ingegneria dell'Automazione. Thesis title: *Implementazione di modelli di machine learning per monocular depth estimation su sistemi embedded*.

- **Andrea Argnani,** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *PULP-Llama2: Modello di linguaggio su architettura embedded a calcolo parallelo ad alta efficienza energetica*.

March 2024 — **Giacomo Saporetti,** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Tecniche di ottimizzazione per applicazioni di apprendimento on-device su architetture Parallel Ultra-Low-Power*.

October 2023 — **Luca Balboni,** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Reti temporali convoluzionali per la previsione di tensioni attuate ad un motore elettrico trifase sincrono a magneti permanenti*.

- **Diego Gorfini,** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Implementation of a Kalman filter-based object tracker on nano-drones*.

February 2023 — **Giulia Kodric',** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Valutazione di algoritmi di object detection per nano-droni*.

December 2022 — **Iacopo Mandrelli,** Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Testing e Valutazione In-Field di un algoritmo di Vision Ranging Fusion per Nano-Quadrotor Autonomi*.

July 2022 — **Anisha Mohamed Sahabdeen,** Ingegneria Informatica. Thesis title: *Tecniche di Deep Learning per Keyword Spotting su Sistemi Embedded*.

Invited Speeches

June 2024 — **The Quest for Open-Source tinyML Heterogeneous Hardware Acceleration: A 10+ Year PULP Journey**, invited keynote speech, tinyML EMEA Innovation Forum, Milano, Italy.

May 2024 — **Open-Source Heterogeneous SoCs for Embedded (and Onboard?) AI Acceleration**, invited speech, Morpheus 2024 ESA workshop on Edge AI and Neuromorphic Hardware Accelerators, ESA ESTEC, Nordwijk, Netherlands.

Invited Speeches (continued)

March 2024
- **Siracusa: a 16nm Extended Reality PULP SoC with Heterogeneous At-MRAM Computing**, invited speech, ADTC and edaWorkshop 24, Dresden, Germany.
- **Advancing the Next Breakthrough in Tiny Smart Robots with Hardware-Accelerated Systems on Chip**, invited speech, ERF TinyML for Tiny Robots workshop, Rimini, Italy.

February 2020
- **Tearing Down the Deep Learning Memory Wall: A Roadmap for Low-Power and High-Performance AI,** International Solid-State Circuits Conference forum "Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking", San Francisco, USA.

Honours & Awards

2024
- **Best Paper Award – IEEE Embedded Vision Workshop** for the 20th IEEE Embedded Vision Workshop (co-located with CVPR 2024): L. Bompani, M. Rusci, D. Palossi, **F. Conti**, and L. Benini, Multi-Resolution Rescored ByteTrack for Video Object Detection on Ultra-low-power Embedded Systems

2021
- **Best Paper Honorable Mention – IEEE International Conference on Application-Specific Architectures and Processors (ASAP)** for L. Bertaccini, L. Benini, **F. Conti**, To Buffer, or Not to Buffer? A Case Study on FFT Accelerators for Ultra-Low-Power Multicore Clusters

2020
- **Darlington Award – IEEE Circuits and Systems Society Best paper award for the IEEE Transactions on Circuits and Systems I: Regular Papers** for **F. Conti**, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, L. Benini, An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics, IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 64, Issue: 9, Sept. 2017, Pages: 2481 - 2494; https://ieee-cas.org/darlington-award

2019
- **Design Contest 2nd Prize – ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)** presented to D. Palossi, **F. Conti**, D. Rossi, L. Benini for PULP-DroNet: Open Source and Open Hardware Artificial Intelligence for Fully Autonomous Navigation on Nano-UAVs

2018
- **Technology Transfer Award – HiPEAC Network of Excellence** awarded to **F. Conti** for the technology transfer project Ultra-Low Energy Hardware Convolution Engine for GAP-8 IoT Application Processor for the successful licensing of an Hardware Intellectual Property (the Hardware Convolution Engine, developed during my PhD and follow-up work) to the French startup GreenWaves Technologies, for usage in their first product GAP-8.
- **Best Paper Award – IEEE CODES+ISSS** for the ESWEEK / CODES+ISSS journal track: **F. Conti**, P. D. Schiavone, L. Benini, XNOR Neural Engine: A Hardware Accelerator IP for 21.6-fJ/op Binary Neural Network Inference, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Volume: 37, Issue: 11, Nov. 2018)

2014
- **Best Paper Award – IEEE Embedded Vision Workshop** for the IEEE Embedded Vision Workshop (co-located with CVPR 2014): **F. Conti**, A. Pullini, L. Benini, Brain-inspired classroom occupancy monitoring on a low-power mobile platform
- **Best Paper Award – IEEE International Conference on Application-Specific Architectures and Processors (ASAP)** for IEEE ASAP 2014: **F. Conti**, C. Pilkington, A. Marongiu, L. Benini, He-P2012: Architectural Heterogeneity Exploration on a Scalable Many-Core Platform

Academic and Authorship Metrics

November 2020 — **Second grade (II fascia) National Scientific Qualification** (art.16 of the law 30 December 2010, n.240) in the Settore Concorsuale 09/E3 (SSD ING-INF/01) - converted to Gruppo Scientifico-Disciplenare 09/IINF-01 - ELETTRONICA (SSD IINF-01/A - Elettronica) as of D.M. 2/5/2024, n. 639.

August 2024 — **h-index** 33 (Google Scholar), 24 (Scopus).

number of citations 3708 (Google Scholar), 2178 (Scopus).

Institutional Activities

Membership of Department Committees

2022 – ongoing — **Teaching Committee (Commissione Didattica)**, CdLM Ing. Elettronica (responsible of student admissions and intakes for the Electronic Engineering master degree course).

Membership of Ph.D. Boards

2023–2024 — **Italian National Ph.D. Programme in Microelectronics**, University of Pavia.

Membership of Final Ph.D. Exam Boards

July 2024 — **Luca Urbinati**, Ph.D. in Ingegneria Elettrica, Elettronica e delle Comunicazioni, Politecnico di Torino.

May 2024 — **Francesco Daghero**, Ph.D. in Ingegneria Informatica e dei Sistemi, Politecnico di Torino.

Membership of Ph.D. Selection Committees

2024 — **PhD Programme on Data Science and Computation** at the University of Bologna, A.Y. 2024/25 – XXXX cycle.

2021 — **PhD Programme on Data Science and Computation** at the University of Bologna, A.Y. 2021/22 – XXXVII cycle.

Membership of Bachelor/Master Graduation Committees

July 2024 — Commissione n. 3 del 22/7/2024 - A.A. 2023/2024 - CdLM Ing. Elettronica.

March 2024 — Commissione n. 3 del 18/3/2024 - A.A. 2023/2024 - CdL Ing. Elettronica e delle Telecomunicazioni, CdLM Ing. Elettronica.

October 2023 — Commissione n. 1 del 14/10/2023 - A.A. 2022/2023 - CdL Ing. Elettronica e delle Telecomunicazioni.

December 2022 — Commissione n. 2 del 5/12/2022 - A.A. 2021/2022 - CdLM Ing. Elettronica.

October 2021 — Commissione n. 8 del 7/10/2021 - A.A. 2020/2021 - CdLM Ing. Elettronica.

July 2021 — Commissione n. 4 del 20/7/2021 - A.A. 2020/2021 - CdL Ing. Elettronica e delle Telecomunicazioni, CdLM Ing. Elettronica.

March 2021 — Commissione n. 6 del 10/3/2021 - A.A. 2019/2020 - CdLM Ing. Elettronica.

Membership of Research Grant Selection Committees

June 2024 — Rep.138/2024 Prot. 2209 del 20/06/2024 - Data-driven and AI-driven approaches for sustainable computing continuum

Institutional Activities (continued)

- Rep.139/2024 Prot. 2211 del 20/06/2024 - Sustainable high-performance computing systems architectures and models

March 2024

- Rep. 57/2024 Prot. 831 del 19/03/2024 - Utilizzo di architetture RISC-V per Migliorare la Sicurezza del Conducente attraverso l'Interazione con i Sistemi ADAS basati su IA
- Rep. 51/2024 Prot. 759 del 14/03/2024 - Development of SW/HW techniques for AI-enhanced Control-Flow-Integrity on Edge

February 2024

- Rep. 42/2024 Prot. 566 del 29/02/2024 - Cluster di Processori RISC-V Riconfigurabili per Elaborazione Per Applicazioni Spaziali

December 2023

- Rep. 309/2023 Prot. 3718 del 18/12/2023 - Performance Evaluation and Optimization of Memory-Centric RISC-V Computing Systems Prototypes
- Rep. 310/2023 Prot. 3720 del 18/12/2023 - Piattaforme cyber-fisiche e di computing continuum per l'environmental monitoring tramite droni autonomi

July 2023

- Rep. 175/2023, Prot. 2123 del 24/07/2023 - Digital Twins technologies for a green computing continuum
- Rep. 178/2023, Prot. 2127 del 24/07/2023 - Development of secure cyberphysical system at the edge

Jun 2023

- Rep. 139/2023, Prot. 1738 del 19/06/2023 - D- SPINER – Digital Twin Applied to Local Sources of Power in Emilia Romagna

February 2023

- Rep. n. 45/2023 Prot. n. 454 del 17/02/2023 - Progettazione Hardware and Software di piattaforma open source a per il controllo in tempo reale

December 2022

- Rep. n. 342/2022 Prot. n. 2827 del 14/12/2022 - Hardware-in-the-Loop framework for optimization of AI applications on edge devices

September 2022

- Rep. 234/2022, Prot. 1987 del 15/09/2022 - Design of energy-efficient and power-aware HPC systems

February 2022

- Rep. 31/2022, Prot. 302 del 14/02/2022 - Hardware-Software Integration of DNN Accelerators for Edge Data Collection and Processing

July 2021

- Rep. n. 59/2021 Prot. n. 477 del 22/07/2021 - Tecniche di apprendimento profondo per segnali audio in applicazioni industriali

March 2021

- Rep. n. 14/2021 Prot. n. 132 del 04/03/2021 - Apprendimento Continuo Online a Precisione Mista in Dispositivi "Extreme Edge"

November 2020

- Rep. n. 64/2020 Prot. n. 566 del 03/11/2020 - Reti neurali profonde su serie temporali per applicazioni industriali

Academic Community Service

2022 – ongoing

- **Associate Editor for IEEE Transactions on Computer-Aided Design of Circuits and Systems**, topic "Architectural Design & Optimization".

2024 – ongoing

- **E3 topic chair (Machine Learning Solutions for Embedded and Cyber-Physical Systems)**, Design, Automation and Test in Europe (DATE) conference (ed. 2025).

2022 – ongoing

- **Member of ESSCIRC / ESSERC technical program committee** (ed. 2023, 2024, 2025).

2019 – 2024

- **Member of SAMOS technical program committee** (ed. 2019 – 2024).

2023

- **E3 topic co-chair (Machine Learning Solutions for Embedded and Cyber-Physical Systems)**, Design, Automation and Test in Europe (DATE) conference (ed. 2024).

Academic Community Service (continued)

2022 — **Chair of TinyML Europe, Middle East and Africa Summit of 2022**, 2nd edition overall and 1st prospective in-person edition.

2021 — **TPC member and TinyHW Track Chair - TinyML Summit**, Burlingame, February 2022.

Co-author of ECS Strategic Research and Innovation Agenda (SRIA) 2022, as co-author of the chapter previously called "Artificial Intelligence, Edge computing, and Advance Control" of the 2022 update to the Electronics Components and Systems Strategic Research and Innovation Agenda (ECS-SRIA), jointly developed by the AENEAS, ARTEMIS-IA and EPoSS industry associations. https://aeneas-office.org/wp-content/uploads/2022/01/ECS-SRIA2022_vb.pdf

2021 – 2022 — **Member of the technical program committee for topic E4 (Design Methodologies for Machine Learning Architectures)**, Design, Automation and Test in Europe (DATE) conference (ed. 2022, 2023).

2017 – 2019 — **Co-Chair of Low-Power Embedded Systems Workshop**, co-located with ACM Computing Frontiers.

Participation to National and International Research Projects

Participation as Principal Investigator

g.a. preparation — **EDF ARCHYTAS**; European Defense Fund project on development of defense-ready innovative AI hardware architectures.

2023 – ongoing — **ISOLDE - High Performance, Safe, Secure, Open-Source Leveraged RISC-V Domain-Specific Ecosystems**; g.a. 101112274; Overall budget € 39410100; Total JU funding € 11582700. The ISOLDE project, funded by the Key Digital Technologies Joint Undertaking of the European Union, is related to domain-specific high-performance RISC-V based systems. I am the Principal Investigator for UNIBO, coordinating all activities from UNIBO within the project.

2022 – 2023 — **iFAB ROADSTER Project**. The ROADSTER project was related to the development of hardware and software to collect vision data for automotive digital twins https://www.ifabfoundation.org/it/project/roadster-road-digital-sustainable-twins-in-emilia-romagna/

Full List of Publications

Journal Articles

1. **F. Conti**, G. Paulin, A. Garofalo, D. Rossi, A. D. Mauro, G. Rutishauser, G. Ottavi, M. Eggimann, H. Okuhara, and L. Benini, "Marsellus: A heterogeneous RISC-V ai-iot end-node soc with 2-8 b DNN acceleration and 30%-boost adaptive body biasing," *IEEE J. Solid State Circuits*, vol. 59, no. 1, pp. 128–142, 2024. DOI: 10.1109/JSSC.2023.3318301.

2. L. Lamberti, L. Bellone, L. Macan, E. Natalizio, **F. Conti**, D. Palossi, and L. Benini, "Distilling tiny and ultra-fast deep neural networks for autonomous navigation on nano-uavs," *IEEE Internet of Things Journal*, 2024. DOI: 10.1109/JIOT.2024.3431913.

3. L. Lamberti, E. Cereda, G. Abbate, L. Bellone, V. J. K. Morinigo, M. Barcis, A. Barcis, A. Giusti, **F. Conti**, and D. Palossi, "A sim-to-real deep learning-based framework for autonomous nano-drone racing," *IEEE Robotics Autom. Lett.*, vol. 9, no. 2, pp. 1899–1906, 2024. DOI: 10.1109/LRA.2024.3349814.

4 A. S. Prasad, M. Scherer, **F. Conti**, D. Rossi, A. D. Mauro, M. Eggimann, J. T. Gómez, Z. Li, S. S. Sarwar, Z. Wang, B. D. Salvo, and L. Benini, "Siracusa: A 16 nm heterogenous RISC-V soc for extended reality with at-mram neural engine," *IEEE J. Solid State Circuits*, vol. 59, no. 7, pp. 2055–2069, 2024. DOI: 10.1109/JSSC.2024.3385987.

5 M. Zanghieri, F. Indirli, A. Latella, G. M. Puglia, F. Tecce, F. Papariello, G. Urlini, L. Benini, and **F. Conti**, "An extreme-edge tcn-based low-latency collision-avoidance safety system for industrial machinery," *IEEE Access*, vol. 12, pp. 16 009–16 021, 2024. DOI: 10.1109/ACCESS.2024.3357510.

6 S. Abadal, R. Guirado, H. Taghvaee, A. Jain, E. P. de Santana, P. H. Bolívar, M. Saeed, R. Negra, Z. Wang, K. Wang, M. C. Lemme, J. Klein, M. Zapater, A. Levisse, D. Atienza, D. Rossi, **F. Conti**, M. Dazzi, G. Karunaratne, I. Boybat, and A. Sebastian, "Graphene-based wireless agile interconnects for massive heterogeneous multi-chip processors," *IEEE Wirel. Commun.*, vol. 30, no. 4, pp. 162–169, 2023. DOI: 10.1109/MWC.010.2100561.

7 D. Nadalini, M. Rusci, L. Benini, and **F. Conti**, "Reduced precision floating-point optimization for deep neural network on-device learning on microcontrollers," *Future Gener. Comput. Syst.*, vol. 149, pp. 212–226, 2023. DOI: 10.1016/J.FUTURE.2023.07.020.

8 G. Ottavi, A. Garofalo, G. Tagliavini, **F. Conti**, A. D. Mauro, L. Benini, and D. Rossi, "Dustin: A 16-cores parallel ultra-low-power cluster with 2b-to-32b fully flexible bit-precision and vector lockstep execution mode," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 70, no. 6, pp. 2450–2463, 2023. DOI: 10.1109/TCSI.2023.3254810.

9 M. Risso, A. Burrello, **F. Conti**, L. Lamberti, Y. Chen, L. Benini, E. Macii, M. Poncino, and D. J. Pagliari, "Lightweight neural architecture search for temporal convolutional networks at the edge," *IEEE Trans. Computers*, vol. 72, no. 3, pp. 744–758, 2023. DOI: 10.1109/TC.2022.3177955.

10 Y. Tortorella, L. Bertaccini, L. Benini, D. Rossi, and **F. Conti**, "Redmule: A mixed-precision matrix-matrix operation engine for flexible and energy-efficient on-chip linear algebra and tinyml training acceleration," *Future Gener. Comput. Syst.*, vol. 149, pp. 122–135, 2023. DOI: 10.1016/J.FUTURE.2023.07.002.

11 A. Garofalo, G. Ottavi, **F. Conti**, G. Karunaratne, I. Boybat, L. Benini, and D. Rossi, "A heterogeneous in-memory computing cluster for flexible end-to-end inference of real-world deep neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 2, pp. 422–435, 2022. DOI: 10.1109/JETCAS.2022.3170152.

12 D. Palossi, N. Zimmerman, A. Burrello, **F. Conti**, H. Müller, L. M. Gambardella, L. Benini, A. Giusti, and J. Guzzi, "Fully onboard ai-powered human-drone pose estimation on ultralow-power autonomous flying nano-uavs," *IEEE Internet Things J.*, vol. 9, no. 3, pp. 1913–1929, 2022. DOI: 10.1109/JIOT.2021.3091643.

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Skills

Languages — **Italian** (mothertongue), **English** (listening: C1, reading: C2, spoken production: C1, spoken interaction: C1, writing: C2).

Coding — **SystemVerilog**, **C**, C++, Bash, Python (+ PyTorch), Rust, …

Misc. — Academic research, teaching, training, consultation, LaTeX typesetting and publishing.