

Francesco Conti

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Employment History

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| September 2022 – current | ■ Senior Assistant Professor (RTD-B) , University of Bologna, Department of Electrical, Electronic, and Information Engineering “Guglielmo Marconi” (DEI). |
| May 2021 – March 2025 (intermittent) | ■ External consultant , ETH Zürich. <i>Development of extreme-edge AI acceleration capabilities for smart glasses, in the context of a collaboration with Meta Reality Labs.</i> |
| May 2020 – September 2024 (intermittent) | ■ External consultant , GreenWaves Technologies. <i>Development of extreme-edge AI acceleration capabilities for wearable audio devices.</i> |
| June 2020 – September 2022 | ■ Junior Assistant Professor (RTD-A) , University of Bologna, Department of Electrical, Electronic, and Information Engineering “Guglielmo Marconi” (DEI). |
| June 2016 – June 2020 | ■ Postdoctoral Researcher , ETH Zürich, Integrated Systems Laboratory, Department of Information Technology and Electrical Engineering (D-ITET). |
| | ■ Research Grant Holder , University of Bologna, Department of Electrical, Electronic, and Information Engineering “Guglielmo Marconi” (DEI). |
| January 2013 – June 2016 | ■ Doctoral Student , University of Bologna, Department of Electrical, Electronic, and Information Engineering “Guglielmo Marconi” (DEI). PhD in “Ingegneria Elettronica, delle Telecomunicazioni e Tecnologie dell’Informazione”, XXVIII cycle. |

Education & Training

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| 2013 – 2016 | ■ Ph.D., University of Bologna in Ingegneria Elettronica, delle Telecomunicazioni e Tecnologie dell’Informazione.
Thesis title: <i>Heterogeneous Architectures for Parallel Acceleration.</i> |
| February – April 2015 | ■ Visiting Ph.D. Student , Stanford University. |
| July – December 2015 | ■ Academic Guest , ETH Zürich. |
| 2010 – 2012 | ■ M.Sc. University of Bologna in Ingegneria Elettronica (110/110 with honours).
Thesis title: <i>Design an Implementation of a Heterogeneous Multicore Shared Memory Cluster for Embedded Computer Vision Applications on FPGA and SoC Platforms.</i> |
| 2008 – 2010 | ■ B.Sc. University of Bologna in Ingegneria Elettronica (110/110 with honours).
Thesis title: <i>Progettazione ed ottimizzazione di readout digitale veloce di sensori a matrice di pixel per la prossima generazione di esperimenti in fisica delle alte energie.</i> |

Teaching Activity

Curricular Teaching Activities at the University of Bologna

- 2022/23 – current  **35364 - Architetture Digitali per l'Elaborazione del Segnale M**, module 1 (3 CFU) for the master degree in Electronic Engineering. Topics: evaluation metrics for digital signal processing architectures, architectural optimization techniques (pipelining, parallelism, multiplexing), design of digital systems for low-power digital signal processing.
- 2021/22 – current  **93398 - Architectures for Artificial Intelligence M**, module 2 (3 CFU) for the master degree in Electronic Engineering. Topics: computational characteristics of Deep Neural Networks (DNNs), DNN quantization, DNN acceleration on large platforms (GPUs) and tiny platforms (microcontrollers), design of advanced hardware accelerators for DNNs.
-  **87198 - Statistics and Architectures for Big Data Processing M**, module 2 (3 CFU) for the master degree in Electronic Engineering; also available as *97467 - Big Data Analytics for Automotive Manufacturing Applications* for the master degree in Advanced Automotive Engineering. Topics: computer architecture, parallel computing, and heterogeneous acceleration techniques.
- 2022/23 – 2023/24  **35364 - Architetture Digitali per l'Elaborazione del Segnale M**, module 1 (3 CFU) for the master degree in Electronic Engineering. Topics: evaluation metrics for digital signal processing architectures, architectural optimization techniques (pipelining, parallelism, multiplexing), design of digital systems for low-power digital signal processing.
-  **91259 - Architecture and Platforms for Artificial Intelligence**, module 3 (1.5 CFU) for the master degree in Artificial Intelligence. Topics: computational characteristics of Deep Neural Networks (DNNs), DNN quantization, DNN acceleration on large platforms (GPUs) and tiny platforms (microcontrollers).
-  **86464 - Algorithms and Systems for Big Data Processing**, module 2 (3 CFU) for the master degree in Advanced Automotive Engineering. Topics: computer architecture, parallel computing, and heterogeneous acceleration techniques.
- 2018/19 – 2019/20  **28651 - Elettronica T-A**, official course tutor for the bachelor degree in Ingegneria Gestionale, course lecturer Prof. A. Bartolini. Topics: basic digital circuits course.

Extra-curricular teaching activities

- June 2024  **Customizing RISC-V Based Microcontrollers**, 18 hours, ETH Future Computing Lab Summer School, Zurich, Switzerland.
- September 2023  **Elements of Machine Learning for Sensor and Edge Computing**, 4 hours, short Ph.D. course for Electronics, Telecommunications, and Information Technology Ph.D. degree, University of Bologna.
- July 2022  **RISC-V: Open ISA, Processors and Systems from AI-enabled IoT to HPC**, 6.25 hours, HiPeAC ACACES Summer School, Fiuggi, Italy.
- July 2019  **Machine Learning Accelerators: from Cloud to Edge**, 3 hours, ACM Summer School, Barcelona, Spain.

Supplementary Teaching Activity & Student Service

Supervision of Ph.D. Students

- Cycle XL  **Andrea Belano**, Italian National Ph.D. degree in Microelectronics, University of Pavia.

Supplementary Teaching Activity & Student Service (continued)

	 Shumaila Sharif , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
Cycle XXXIX	 Alessandro Nadalini , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
Cycle XXXVIII	 Luka Macan , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.  Luca Bompani , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
Cycle XXXVII	 Yvan Tortorella , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.  Mahyar Pourjabar , Ph.D. degree in Data Science and Computation, University of Bologna, University of Bologna.

Co-Supervision of Ph.D. Students

ongoing	 Philip Wiese , Doctor of Science at ETH Zürich.  Victor Jung , Doctor of Science at ETH Zürich.  Gamze Islamoglu , Doctor of Science at ETH Zürich.  Arpan Prasad , Doctor of Science at ETH Zürich.
2024	 Georg Rutishauser , Doctor of Science at ETH Zürich.  Gianna Paulin , Doctor of Science at ETH Zürich.
Cycle XL	 Riccardo Fiorani Gallotta , Italian National Ph.D. degree in Microelectronics, University of Pavia.
Cycle XXXIX	 Riccardo Tedeschi , Ph.D. degree in Electronics, Telecommunications and Information Technology, University of Bologna.
Cycle XXXVII	 Davide Nadalini , Italian National Ph.D. degree in Artificial Intelligence, Politecnico di Torino.  Alberto Dequino , Italian National Ph.D. degree in Artificial Intelligence, Politecnico di Torino.

Supervision of Master Theses

March 2025	 Ilenia Carboni , Artificial Intelligence. Thesis title: <i>Federated Neural Radiance Fields on a Swarm of Miniaturized Robots</i> .  Taha El Bayad , Electronic Engineering. Thesis title: <i>Simulation and Deployment Support for Transformers on Snitch-based RISC-V Hardware Accelerator</i> .  Lorenzo Grandi , Electronic Engineering. Thesis title: <i>Self-learning AI-driven FOC for ARCP based traction inverter</i> .  Giovanni Oltrecolli , Electronic Engineering. Thesis title: <i>Neural Networks-Based MVDR Beamforming for Real-Time Speech Enhancement on an Ultra-Low Power Microcontroller</i> .
December 2024	 Călin Diaconu , Artificial Intelligence. Thesis title: <i>Latent Replay-Based On-Device Continual Learning Using Transformers on Edge, Ultra-Low-Power IoT Platforms</i> .  Manuel Sanchini , Electronic Engineering. Thesis title: <i>Autoapprendimento non supervisionato end-to-end di una rete neurale per object detection</i> .
July 2024	 Andrea Belano , Computer Engineering. Thesis title: <i>Softex: Softmax Computing Engine for Fast Exponential Acceleration</i> .

Supplementary Teaching Activity & Student Service (continued)

- March 2024  **Luca Angeli**, Electronic Engineering. Thesis title: *Progetto di hardware per la conversione di protocolli applicato a sensori di immagini basati su eventi.*
-  **Stefano Di Labio**, Electronic Engineering. Thesis title: *A Survey of Techniques and Architectures for Extended Reality Computing.*
-  **Luigi Ghionda**, Electronic Engineering. Thesis title: *Design of a Multi-Precision Floating-Point FFT Hardware Accelerator.*
-  **Athar Zafeer Kannamangalam Aslam Basha**, Electronic Engineering. Thesis title: *Automatic insertion of fault-injectable flip-flops in FPGA emulators of computing platforms.*
- February 2024  **Aurora Di Giampietro**, Electronic Engineering. Thesis title: *Integrating a Tensor Datapath into a Small and Efficient Vector Processor.*
- March 2023  **Michele Gaspari**, Computer Science. Thesis title: *Multi Source Speech Enhancement for Low-Power Micro-Controller devices.*
- October 2022  **Luca Bompani**, Artificial Intelligence. Thesis title: *Embedding Video Object Detection Capabilities on Low-Power Nano-Drones.*
-  **Mattia Orlandi**, Artificial Intelligence. Thesis title: *Motor Unit Spike Trains Reconstruction from sEMG Signals for Gesture Classification on a Low-Power Processing Platform.*
-  **Angely Jazmín Oyola Suarez**, Artificial Intelligence. Thesis title: *An Embedded In-Cabin Lightweight High-Performance 3D Gaze Estimation System.*
- July 2022  **Pierangelo Maria Rapa**, Electronic Engineering. Thesis title: *Design of a wearable platform for PPG analysis with multicore low-power processor.*
- October 2021  **Pietro Maltoni**, Electronic Engineering. Thesis title: *Progetto di un acceleratore hardware per layer di convoluzioni depthwise in applicazioni di Deep Neural Network.*
-  **Hossein Shirali**, Electronic Engineering. Thesis title: *Semi-Automatic Image Labeling Method Based On Point Clouds.*
-  **Yvan Tortorella**, Electronic Engineering. Thesis title: *Design of a Low-Precision Floating-Point Matrix Multiplication Accelerator for On-Chip Deep Learning.*
- July 2021  **Manuel Cintura**, Advanced Automotive Electronic Engineering. Thesis title: *An Embedded Data Logger for In-Vehicle Testing.*
-  **Riccardo Gandolfi**, Electronic Engineering. Thesis title: *Design of a memory-to-memory tensor reshuffle unit for ultra-low-power deep learning accelerators.*
-  **Mahyar Pourjabar**, Electronic Engineering. Thesis title: *Federated Continual Learning for Distributed Deep-Edge Devices.*
- March 2021  **Davide Nadalini**, Electronic Engineering. Thesis title: *Mixed Precision Online Learning on a Parallel Ultra-Low Power Platform.*

Co-Supervision of Master Theses

- March 2024  **Lorenzo Greco**, Electronic Engineering. Thesis title: *Progettazione di un cluster eterogeneo con acceleratore analogico per intelligenza artificiale basato su ePCM.*
- October 2021  **Alessandro Nadalini**, Electronic Engineering. Thesis title: *Progettazione ed ottimizzazione di un processore dedicato per accelerazione di reti neurali quantizzate a precisione mista.*
- July 2021  **Mattia Sinigaglia**, Computer Engineering. Thesis title: *Progettazione ed implementazione di un Sistema On Chip per applicazioni audio.*

Supplementary Teaching Activity & Student Service (continued)

Supervision of Bachelor Theses

- July 2024  **Antonio D'Alessandro**, Ingegneria dell'Automazione. Thesis title: *Implementazione di modelli di machine learning per monocular depth estimation su sistemi embedded*.
-  **Andrea Argnani**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *PULP-Llamaz: Modello di linguaggio su architettura embedded a calcolo parallelo ad alta efficienza energetica*.
- March 2024  **Giacomo Saporetti**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Tecniche di ottimizzazione per applicazioni di apprendimento on-device su architetture Parallel Ultra-Low-Power*.
- October 2023  **Luca Balboni**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Reti temporali convoluzionali per la previsione di tensioni attuate ad un motore elettrico trifase sincrono a magneti permanenti*.
-  **Diego Gorfini**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Implementation of a Kalman filter-based object tracker on nano-drones*.
- February 2023  **Giulia Kodric**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Valutazione di algoritmi di object detection per nano-droni*.
- December 2022  **Iacopo Mandrelli**, Ingegneria Elettronica e delle Telecomunicazioni. Thesis title: *Testing e Valutazione In-Field di un algoritmo di Vision Ranging Fusion per Nano-Quadrotor Autonomi*.
- July 2022  **Anisha Mohamed Sahabdeen**, Ingegneria Informatica. Thesis title: *Tecniche di Deep Learning per Keyword Spotting su Sistemi Embedded*.

Invited Speeches

- October 2024  **The Quest for Open-Source tinyML Heterogeneous Hardware Acceleration: A 10+ Year PULP Journey**, invited speech, EU-India Joint Researchers Workshop on Semiconductors, Brussels, Belgium.
- June 2024  **The Quest for Open-Source tinyML Heterogeneous Hardware Acceleration: A 10+ Year PULP Journey**, invited keynote speech, tinyML EMEA Innovation Forum, Milano, Italy.
- May 2024  **Open-Source Heterogeneous SoCs for Embedded (and Onboard?) AI Acceleration**, invited speech, Morpheus 2024 ESA workshop on Edge AI and Neuromorphic Hardware Accelerators, ESA ESTEC, Noordwijk, Netherlands.
- March 2024  **Siracusa: a 16nm Extended Reality PULP SoC with Heterogeneous At-MRAM Computing**, invited speech, ADTC and edaWorkshop 24, Dresden, Germany.
-  **Advancing the Next Breakthrough in Tiny Smart Robots with Hardware-Accelerated Systems on Chip**, invited speech, ERF TinyML for Tiny Robots workshop, Rimini, Italy.
- February 2020  **Tearing Down the Deep Learning Memory Wall: A Roadmap for Low-Power and High-Performance AI**, International Solid-State Circuits Conference forum "Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking", San Francisco, USA.

Honours & Awards

- 2024  **IEEE - Elevation to "Senior Member" grade.**

Honours & Awards (continued)

- 2023  **Best Paper Award – IEEE Embedded Vision Workshop** for the 20th IEEE Embedded Vision Workshop (co-located with CVPR 2024): L. Bompani, M. Rusci, D. Palossi, **F. Conti**, and L. Benini, *Multi-Resolution Rescored ByteTrack for Video Object Detection on Ultra-low-power Embedded Systems*.
- 2021  **Best Paper Award - IEEE Computer Society Annual Symposium on VLSI (ISVLSI)** for A. Nadalini, G. Rutishauser, A. Burrello, N. Bruschi, A. Garofalo, L. Benini, **F. Conti**, D. Rossi, *A 3 TOPS/W RISC-V parallel cluster for inference of fine-grain mixed-precision quantized neural networks*.
- 2021  **Best Paper Honorable Mention – IEEE International Conference on Application-Specific Architectures and Processors (ASAP)** for L. Bertaccini, L. Benini, **F. Conti**, *To Buffer, or Not to Buffer? A Case Study on FFT Accelerators for Ultra-Low-Power Multicore Clusters*
- 2020  **Darlington Award – IEEE Circuits and Systems Society Best paper award for the IEEE Transactions on Circuits and Systems I: Regular Papers** for **F. Conti**, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, L. Benini, *An IoT Endpoint System-on-Chip for Secure and Energy-Efficient Near-Sensor Analytics*, IEEE Transactions on Circuits and Systems I: Regular Papers, Volume: 64, Issue: 9, Sept. 2017, Pages: 2481 - 2494;  <https://iee-cas.org/darlington-award>
- 2019  **Design Contest 2nd Prize – ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED)** presented to D. Palossi, **F. Conti**, D. Rossi, L. Benini for *PULP-DroNet: Open Source and Open Hardware Artificial Intelligence for Fully Autonomous Navigation on Nano-UAVs*
- 2018  **Technology Transfer Award – HiPEAC Network of Excellence** awarded to **F. Conti** for the technology transfer project *Ultra-Low Energy Hardware Convolution Engine for GAP-8 IoT Application Processor* for the successful licensing of an Hardware Intellectual Property (the Hardware Convolution Engine, developed during my PhD and follow-up work) to the French startup GreenWaves Technologies, for usage in their first product GAP-8.
-  **Best Paper Award – IEEE CODES+ISSS** for the ESWEEK / CODES+ISSS journal track: **F. Conti**, P. D. Schiavone, L. Benini, *XNOR Neural Engine: A Hardware Accelerator IP for 21.6-fj/op Binary Neural Network Inference*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Volume: 37, Issue: 11, Nov. 2018)
- 2014  **Best Paper Award – IEEE Embedded Vision Workshop** for the IEEE Embedded Vision Workshop (co-located with CVPR 2014): **F. Conti**, A. Pullini, L. Benini, *Brain-inspired classroom occupancy monitoring on a low-power mobile platform*
-  **Best Paper Award – IEEE International Conference on Application-Specific Architectures and Processors (ASAP)** for IEEE ASAP 2014: **F. Conti**, C. Pilkington, A. Marongiu, L. Benini, *He-P2012: Architectural Heterogeneity Exploration on a Scalable Many-Core Platform*

Academic and Authorship Metrics

- November 2020  **Second grade (II fascia) National Scientific Qualification** (art.16 of the law 30 December 2010, n.240) in the Settore Concorsuale 09/E3 (SSD ING-INF/01) - converted to Gruppo Scientifico-Disciplinare 09/IINF-01 - ELETTRONICA (SSD IINF-01/A - Elettronica) as of D.M. 2/5/2024, n. 639.
- March 2025  **h-index** 36 (Google Scholar), 27 (Scopus).
-  **number of citations** 4427 (Google Scholar), 2626 (Scopus).

Institutional Activities

Membership of Department Committees

- 2022 – ongoing  **Teaching Committee (Commissione Didattica)**, CdLM Ing. Elettronica (responsible of student admissions and intakes for the Electronic Engineering master degree course).

Membership of Ph.D. Boards

- 2023–2024  **Italian National Ph.D. Programme in Microelectronics**, University of Pavia.

Membership of Final Ph.D. Exam Boards

- July 2024  **Luca Urbinati**, Ph.D. in Ingegneria Elettrica, Elettronica e delle Comunicazioni, Politecnico di Torino.
- May 2024  **Francesco Daghero**, Ph.D. in Ingegneria Informatica e dei Sistemi, Politecnico di Torino.

Membership of Ph.D. Selection Committees

- 2024  **PhD Programme on Data Science and Computation** at the University of Bologna, A.Y. 2024/25 – XXXX cycle.
- 2021  **PhD Programme on Data Science and Computation** at the University of Bologna, A.Y. 2021/22 – XXXVII cycle.

Membership of Bachelor/Master Graduation Committees

- December 2024  Commissione n. 9 del 4/12/2024 - A.A. 2023/2024 - CdLM Ing. Elettronica.
- July 2024  Commissione n. 3 del 22/7/2024 - A.A. 2023/2024 - CdLM Ing. Elettronica.
- March 2024  Commissione n. 3 del 18/3/2024 - A.A. 2023/2024 - CdL Ing. Elettronica e delle Telecomunicazioni, CdLM Ing. Elettronica.
- October 2023  Commissione n. 1 del 14/10/2023 - A.A. 2022/2023 - CdL Ing. Elettronica e delle Telecomunicazioni.
- December 2022  Commissione n. 2 del 5/12/2022 - A.A. 2021/2022 - CdLM Ing. Elettronica.
- October 2021  Commissione n. 8 del 7/10/2021 - A.A. 2020/2021 - CdLM Ing. Elettronica.
- July 2021  Commissione n. 4 del 20/7/2021 - A.A. 2020/2021 - CdL Ing. Elettronica e delle Telecomunicazioni, CdLM Ing. Elettronica.
- March 2021  Commissione n. 6 del 10/3/2021 - A.A. 2019/2020 - CdLM Ing. Elettronica.

Membership of Research Grant Selection Committees

- June 2024  Rep.138/2024 Prot. 2209 del 20/06/2024 - Data-driven and AI-driven approaches for sustainable computing continuum
-  Rep.139/2024 Prot. 2211 del 20/06/2024 - Sustainable high-performance computing systems architectures and models
- March 2024  Rep. 57/2024 Prot. 831 del 19/03/2024 - Utilizzo di architetture RISC-V per Migliorare la Sicurezza del Conducente attraverso l'Interazione con i Sistemi ADAS basati su IA
-  Rep. 51/2024 Prot. 759 del 14/03/2024 - Development of SW/HW techniques for AI-enhanced Control-Flow-Integrity on Edge
- February 2024  Rep. 42/2024 Prot. 566 del 29/02/2024 - Cluster di Processori RISC-V Riconfigurabili per Elaborazione Per Applicazioni Spaziali

Institutional Activities (continued)

December 2023	Rep. 309/2023 Prot. 3718 del 18/12/2023 - Performance Evaluation and Optimization of Memory-Centric RISC-V Computing Systems Prototypes
	Rep. 310/2023 Prot. 3720 del 18/12/2023 - Piattaforme cyber-fisiche e di computing continuum per l'environmental monitoring tramite droni autonomi
July 2023	Rep. 175/2023, Prot. 2123 del 24/07/2023 - Digital Twins technologies for a green computing continuum
	Rep. 178/2023, Prot. 2127 del 24/07/2023 - Development of secure cyberphysical system at the edge
Jun 2023	Rep. 139/2023, Prot. 1738 del 19/06/2023 - D- SPINER – Digital Twin Applied to Local Sources of Power in Emilia Romagna
February 2023	Rep. n. 45/2023 Prot. n. 454 del 17/02/2023 - Progettazione Hardware and Software di piattaforma open source a per il controllo in tempo reale
December 2022	Rep. n. 342/2022 Prot. n. 2827 del 14/12/2022 - Hardware-in-the-Loop framework for optimization of AI applications on edge devices
September 2022	Rep. 234/2022, Prot. 1987 del 15/09/2022 - Design of energy-efficient and power-aware HPC systems
February 2022	Rep. 31/2022, Prot. 302 del 14/02/2022 - Hardware-Software Integration of DNN Accelerators for Edge Data Collection and Processing
July 2021	Rep. n. 59/2021 Prot. n. 477 del 22/07/2021 - Tecniche di apprendimento profondo per segnali audio in applicazioni industriali
March 2021	Rep. n. 14/2021 Prot. n. 132 del 04/03/2021 - Apprendimento Continuo Online a Precisione Mista in Dispositivi “Extreme Edge”
November 2020	Rep. n. 64/2020 Prot. n. 566 del 03/11/2020 - Reti neurali profonde su serie temporali per applicazioni industriali

Academic Community Service

2025 – ongoing	Member of ISSCC technical program committee (ed. 2026), Digital Architecture & Systems sub-committee.
2022 – ongoing	Associate Editor for IEEE Transactions on Computer-Aided Design of Circuits and Systems , topic “Architectural Design & Optimization”.
2024 – ongoing	E3 topic chair (Machine Learning Solutions for Embedded and Cyber-Physical Systems) , Design, Automation and Test in Europe (DATE) conference (ed. 2025).
2024	ESSERC 2024 session chair . Track A2L-B (Digital Compute-in-Memory for ML).
2022 – ongoing	Member of ESSCIRC / ESSERC technical program committee (ed. 2023, 2024, 2025).
2019 – 2024	Member of SAMOS technical program committee (ed. 2019 – 2024).
2022 – ongoing	Sponsorship chair , ACM Computing Frontiers (ed. 2023 – 2025).
2023	E3 topic co-chair (Machine Learning Solutions for Embedded and Cyber-Physical Systems) , Design, Automation and Test in Europe (DATE) conference (ed. 2024).
2022	General Chair of TinyML Europe, Middle East and Africa (EMEA) Innovation Forum , Limassol, Cyprus, October 2022.
2021	TPC member and TinyHW Track Chair - TinyML Summit , Burlingame, California, February 2022.

Academic Community Service (continued)

- 2021–ongoing  **Co-author of ECS Strategic Research and Innovation Agenda (SRIA) 2022**, as co-author of the chapter previously called "Artificial Intelligence, Edge computing, and Advance Control" of the 2022 update to the Electronics Components and Systems Strategic Research and Innovation Agenda (ECS-SRIA), jointly developed by the AENEAS, ARTEMIS-IA and EPoSS industry associations.  https://aeneas-office.org/wp-content/uploads/2022/01/ECS-SRIA2022_vb.pdf
- 2021 – 2022  **Member of the technical program committee for topic E4 (Design Methodologies for Machine Learning Architectures)**, Design, Automation and Test in Europe (DATE) conference (ed. 2022, 2023).
- 2017 – 2019  **Co-Chair of Low-Power Embedded Systems Workshop**, co-located with ACM Computing Frontiers.

Participation to National, International and Industrial Projects

Participation as Scientific Lead in National and International Projects

- 2025 – ongoing  **SNSF RoboMix²**; Swiss National Science Foundation project on mixed event/frame-based on-device learning on mixed spiking artificial neural networks for robotics; Overall budget CHF 1'632'479; g.a. 200021-236595. I am the scientific lead (responsabile scientifico) for UNIBO.
- 2024 – ongoing  **EDF ARCHYTAS**; European Defense Fund project on development of defense-ready innovative AI hardware architectures; Overall budget € 19'976'637. I am the scientific lead (responsabile scientifico) for UNIBO and the leader of WP5 (System and Software).
- 2023 – ongoing  **ISOLDE - High Performance, Safe, Secure, Open-Source Leveraged RISC-V Domain-Specific Ecosystems**; g.a. 10112274; Overall budget € 39'410'100; Total JU funding € 11'582'700. The ISOLDE project, funded by the Key Digital Technologies Joint Undertaking of the European Union, is related to domain-specific high-performance RISC-V based systems. I am the scientific lead (responsabile scientifico) for UNIBO, coordinating all activities from UNIBO within the project.
- 2022 – 2023  **iFAB ROADSTER Project**. The ROADSTER project was related to the development of hardware and software to collect vision data for automotive digital twins  <https://www.ifabfoundation.org/it/project/roadster-road-digital-sustainable-twins-in-emilia-romagna/>

Participation as Member of the Research Team in National and International Projects

- 2022 – ongoing  **National Centre for HPC, Big Data and Quantum Computing, Spoke 1: Future HPC**; Piano Nazionale di Ripresa e Resilienza (PNRR). I am the primary UNIBO contact for the activities of Flagship 2 on acceleration architectures.
-  **NeuroSoC - A multiprocessor system-on-chip with in-memory neural processing unit**; g.a. 101070634; Total EU funding € 7'952'677. The project, whose PI is Prof. Eleonora Franchi Scarselli, deals with the development of an innovative SoC including both digital processing and analog in-memory-computing capabilities. I am a member of the research team for UNIBO, responsible of all activities related to digital design (WP3) and software development (WP4), which constitute ~50% of UNIBO's effort in the project.

Participation to National, International and Industrial Projects (continued)

- 2021 – ongoing  **The European Pilot**; g.a. 101034126; Total EU funding € 14'999'962. I collaborate on activities related to the design of RISC-V based VEC and MLP chips.
- 2019 – 2023  **AI4DI - Artificial Intelligence for Digitizing Industry**; g.a. 826060; total EU funding €8'763'190. With the University of Bologna, I have been a member of the UNIBO research team for the ECSEL AI4DI project (2019-ongoing), to which UNIBO participated through the IUNET consortium. I have been the main contact of UNIBO with respect to the project and the leader of task T4.1. UNIBO's contribution focuses on the development of ultra-low-power DNN-based algorithms for enhanced worker safety of industrial woodworking machinery.
- 2018 – 2020  **ALOHA – software framework for runtime-Adaptive and secure deep Learning On Heterogeneous Architectures**; g.a. 780788; total EU funding € 5'976'415. While working as a post-doctoral researcher at ETH Zurich, I have been Work Package leader for WP2 in the EU H2020 ALOHA project (2018–2020). The work package focused on the design of a framework for neural architecture search of topologies distilled for secure execution on embedded devices; ETH's contribution is on network quantization and resulted in the open-source NEMO project (<https://github.com/pulp-platform/nemo>).

Participation as Member of the Research Team in Industrial Projects

- 2021 – ongoing  **Meta Reality Labs collaboration**. In the capacity of external consultant to ETH Zürich, I participate to the scientific activities of an ongoing cooperation between ETH and Meta Reality Labs (USA), for the development of state-of-the-art RISC-V based AI acceleration architectures for wearable devices, in particular smart and extended reality (XR) glasses.

Full List of Publications

Journal Articles

- 1 A. Dequino, L. Bompani, L. Benini, and **F. Conti**, “Optimizing bfloat16 deployment of tiny transformers on ultra-low power extreme edge socs,” *Journal of Low Power Electronics and Applications*, vol. 15, no. 1, 2025, ISSN: 2079-9268.  DOI: 10.3390/jlpea15010008.
- 2 V. J. Jung, A. Burrello, M. Scherer, **F. Conti**, and L. Benini, “Optimizing the deployment of tiny transformers on low-power mcus,” *IEEE Trans. Computers*, vol. 74, no. 2, pp. 526–541, 2025.  DOI: 10.1109/TC.2024.3500360.
- 3 M. Rogenmoser, Y. Tortorella, D. Rossi, **F. Conti**, and L. Benini, “Hybrid modular redundancy: Exploring modular redundancy approaches in RISC-V multi-core computing clusters for reliable processing in space,” *ACM Trans. Cyber Phys. Syst.*, vol. 9, no. 1, 8:1–8:29, 2025.  DOI: 10.1145/3635161.
- 4 **F. Conti**, G. Paulin, A. Garofalo, D. Rossi, A. D. Mauro, G. Rutishauser, G. Ottavi, M. Eggimann, H. Okuhara, and L. Benini, “Marsellus: A heterogeneous RISC-V ai-iot end-node soc with 2-8 b DNN acceleration and 30%-boost adaptive body biasing,” *IEEE J. Solid State Circuits*, vol. 59, no. 1, pp. 128–142, 2024.  DOI: 10.1109/JSSC.2023.3318301.
- 5 L. Lamberti, L. Bellone, L. Macan, E. Natalizio, **F. Conti**, D. Palossi, and L. Benini, “Distilling tiny and ultra-fast deep neural networks for autonomous navigation on nano-uavs,” *IEEE Internet of Things Journal*, 2024.  DOI: 10.1109/JIOT.2024.3431913.

- 6 L. Lamberti, E. Cereda, G. Abbate, L. Bellone, V. J. K. Morinigo, M. Barcis, A. Barcis, A. Giusti, **F. Conti**, and D. Palossi, "A sim-to-real deep learning-based framework for autonomous nano-drone racing," *IEEE Robotics Autom. Lett.*, vol. 9, no. 2, pp. 1899–1906, 2024.  DOI: 10.1109/LRA.2024.3349814.
- 7 A. S. Prasad, M. Scherer, **F. Conti**, D. Rossi, A. D. Mauro, M. Eggimann, J. T. Gómez, Z. Li, S. S. Sarwar, Z. Wang, B. D. Salvo, and L. Benini, "Siracusa: A 16 nm heterogenous RISC-V soc for extended reality with at-mram neural engine," *IEEE J. Solid State Circuits*, vol. 59, no. 7, pp. 2055–2069, 2024.  DOI: 10.1109/JSSC.2024.3385987.
- 8 M. Scherer, L. Macan, V. J. B. Jung, P. Wiese, L. Bompani, A. Burrello, **F. Conti**, and L. Benini, "Deeploy: Enabling energy-efficient deployment of small language models on heterogeneous microcontrollers," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 43, no. 11, pp. 4009–4020, 2024.  DOI: 10.1109/TCAD.2024.3443718.
- 9 M. Zanghieri, F. Indirli, A. Latella, G. M. Puglia, F. Tecce, F. Papariello, G. Urlini, L. Benini, and **F. Conti**, "An extreme-edge tcnn-based low-latency collision-avoidance safety system for industrial machinery," *IEEE Access*, vol. 12, pp. 16 009–16 021, 2024.  DOI: 10.1109/ACCESS.2024.3357510.
- 10 S. Abadal, R. Guirado, H. Taghvaei, A. Jain, E. P. de Santana, P. H. Bolívar, M. Saeed, R. Negra, Z. Wang, K. Wang, M. C. Lemme, J. Klein, M. Zapater, A. Levisse, D. Atienza, D. Rossi, **F. Conti**, M. Dazzi, G. Karunaratne, I. Boybat, and A. Sebastian, "Graphene-based wireless agile interconnects for massive heterogeneous multi-chip processors," *IEEE Wirel. Commun.*, vol. 30, no. 4, pp. 162–169, 2023.  DOI: 10.1109/MWC.010.2100561.
- 11 D. Nadalini, M. Rusci, L. Benini, and **F. Conti**, "Reduced precision floating-point optimization for deep neural network on-device learning on microcontrollers," *Future Gener. Comput. Syst.*, vol. 149, pp. 212–226, 2023.  DOI: 10.1016/J.FUTURE.2023.07.020.
- 12 G. Ottavi, A. Garofalo, G. Tagliavini, **F. Conti**, A. D. Mauro, L. Benini, and D. Rossi, "Dustin: A 16-cores parallel ultra-low-power cluster with 2b-to-32b fully flexible bit-precision and vector lockstep execution mode," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 70, no. 6, pp. 2450–2463, 2023.  DOI: 10.1109/TCSI.2023.3254810.
- 13 M. Risso, A. Burrello, **F. Conti**, L. Lamberti, Y. Chen, L. Benini, E. Macii, M. Poncino, and D. J. Pagliari, "Lightweight neural architecture search for temporal convolutional networks at the edge," *IEEE Trans. Computers*, vol. 72, no. 3, pp. 744–758, 2023.  DOI: 10.1109/TC.2022.3177955.
- 14 Y. Tortorella, L. Bertaccini, L. Benini, D. Rossi, and **F. Conti**, "Redmule: A mixed-precision matrix-matrix operation engine for flexible and energy-efficient on-chip linear algebra and tinyml training acceleration," *Future Gener. Comput. Syst.*, vol. 149, pp. 122–135, 2023.  DOI: 10.1016/J.FUTURE.2023.07.002.
- 15 A. Garofalo, G. Ottavi, **F. Conti**, G. Karunaratne, I. Boybat, L. Benini, and D. Rossi, "A heterogeneous in-memory computing cluster for flexible end-to-end inference of real-world deep neural networks," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 12, no. 2, pp. 422–435, 2022.  DOI: 10.1109/JETCAS.2022.3170152.
- 16 D. Palossi, N. Zimmerman, A. Burrello, **F. Conti**, H. Müller, L. M. Gambardella, L. Benini, A. Giusti, and J. Guzzi, "Fully onboard ai-powered human-drone pose estimation on ultralow-power autonomous flying nano-uavs," *IEEE Internet Things J.*, vol. 9, no. 3, pp. 1913–1929, 2022.  DOI: 10.1109/JIOT.2021.3091643.
- 17 G. Paulin, **F. Conti**, L. Cavigelli, and L. Benini, "Vau da muntanialas: Energy-efficient multi-die scalable acceleration of RNN inference," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 69, no. 1, pp. 244–257, 2022.  DOI: 10.1109/TCSI.2021.3099716.
- 18 D. Rossi, **F. Conti**, M. Eggimann, A. D. Mauro, G. Tagliavini, S. Mach, M. Guermandi, A. Pullini, I. Loi, J. Chen, E. Flamand, and L. Benini, "Vega: A ten-core soc for iot endnodes with DNN acceleration and

- cognitive wake-up from mram-based state-retentive sleep mode," *IEEE J. Solid State Circuits*, vol. 57, no. 1, pp. 127–139, 2022.  DOI: 10.1109/JSSC.2021.3114881.
- 19 A. Burrello, A. Garofalo, N. Bruschi, G. Tagliavini, D. Rossi, and **F. Conti**, "DORY: automatic end-to-end deployment of real-world dnns on low-cost iot mcus," *IEEE Trans. Computers*, vol. 70, no. 8, pp. 1253–1268, 2021.  DOI: 10.1109/TC.2021.3066883.
 - 20 A. Garofalo, G. Tagliavini, **F. Conti**, L. Benini, and D. Rossi, "Xpulpnn: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based iot end nodes," *IEEE Trans. Emerg. Top. Comput.*, vol. 9, no. 3, pp. 1489–1505, 2021.  DOI: 10.1109/TETC.2021.3072337.
 - 21 V. Niculescu, L. Lamberti, **F. Conti**, L. Benini, and D. Palossi, "Improving autonomous nano-drones performance via automated end-to-end optimization and deployment of dnns," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 11, no. 4, pp. 548–562, 2021.  DOI: 10.1109/JETCAS.2021.3126259.
 - 22 G. Paulin, R. Andri, **F. Conti**, and L. Benini, "Rnn-based radio resource management on multicore RISC-V accelerator architectures," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 29, no. 9, pp. 1624–1637, 2021.  DOI: 10.1109/TVLSI.2021.3093242.
 - 23 L. Ravaglia, M. Rusci, D. Nadalini, A. Capotondi, **F. Conti**, and L. Benini, "A tinymml platform for on-device continual learning with quantized latent replays," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 11, no. 4, pp. 789–802, 2021.  DOI: 10.1109/JETCAS.2021.3121554.
 - 24 A. D. Mauro, **F. Conti**, P. D. Schiavone, D. Rossi, and L. Benini, "Always-on 674 μ w@4gop/s error resilient binary neural networks with aggressive SRAM voltage scaling on a 22-nm iot end-node," *IEEE Trans. Circuits Syst.*, vol. 67-I, no. 11, pp. 3905–3918, 2020.  DOI: 10.1109/TCSI.2020.3012576.
 - 25 P. Meloni, D. Loi, G. Deriu, M. Carreras, **F. Conti**, A. Capotondi, and D. Rossi, "Exploring neuraghe: A customizable template for apsoc-based CNN inference at the edge," *IEEE Embed. Syst. Lett.*, vol. 12, no. 2, pp. 62–65, 2020.  DOI: 10.1109/LES.2019.2947312.
 - 26 T. Serrano-Gotarredona, M. Valle, **F. Conti**, and H. Li, "Introduction to the special issue on the 2nd IEEE international conference on artificial intelligence circuits and systems (AICAS 2020)," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 10, no. 4, pp. 403–405, 2020.  DOI: 10.1109/JETCAS.2020.3040581.
 - 27 M. Zanghieri, S. Benatti, A. Burrello, V. J. Kartsch, **F. Conti**, and L. Benini, "Robust real-time embedded EMG recognition framework using temporal convolutional networks on a multicore iot processor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 2, pp. 244–256, 2020.  DOI: 10.1109/TBCAS.2019.2959160.
 - 28 D. Palossi, A. Loquercio, **F. Conti**, E. Flamand, D. Scaramuzza, and L. Benini, "A 64-mw dnn-based visual navigation engine for autonomous nano-drones," *IEEE Internet Things J.*, vol. 6, no. 5, pp. 8357–8371, 2019.  DOI: 10.1109/JIOT.2019.2917066.
 - 29 **F. Conti**, P. D. Schiavone, and L. Benini, "XNOR neural engine: A hardware accelerator IP for 21.6-fj/op binary neural network inference," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 37, no. 11, pp. 2940–2951, 2018.  DOI: 10.1109/TCAD.2018.2857019.
 - 30 P. Meloni, A. Capotondi, G. Deriu, M. Brian, **F. Conti**, D. Rossi, L. Raffo, and L. Benini, "Neuraghe: Exploiting CPU-FPGA synergies for efficient and flexible CNN inference acceleration on zynq socs," *ACM Trans. Reconfigurable Technol. Syst.*, vol. 11, no. 3, 18:1–18:24, 2018.  DOI: 10.1145/3284357.
 - 31 A. Pullini, **F. Conti**, D. Rossi, I. Loi, M. Gautschi, and L. Benini, "A heterogeneous multicore system on chip for energy efficient brain inspired computing," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 65-II, no. 8, pp. 1094–1098, 2018.  DOI: 10.1109/TCSII.2017.2652982.
 - 32 **F. Conti**, D. Palossi, R. Andri, M. Magno, and L. Benini, "Accelerated visual context classification on a low-power smartwatch," *IEEE Trans. Hum. Mach. Syst.*, vol. 47, no. 1, pp. 19–30, 2017.  DOI: 10.1109/THMS.2016.2623482.

- 33 **F. Conti**, R. Schilling, P. D. Schiavone, A. Pullini, D. Rossi, F. K. Gürkaynak, M. Muehlberghuber, M. Gautschi, I. Loi, G. Haugou, S. Mangard, and L. Benini, "An iot endpoint system-on-chip for secure and energy-efficient near-sensor analytics," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 64-I, no. 9, pp. 2481–2494, 2017.  DOI: 10.1109/TCSI.2017.2698019.
- 34 D. Rossi, I. Loi, A. Pullini, T. C. Müller, A. Burg, **F. Conti**, L. Benini, and P. Flatresse, "A self-aware architecture for PVT compensation and power nap in near threshold processors," *IEEE Des. Test*, vol. 34, no. 6, pp. 46–53, 2017.  DOI: 10.1109/MDAT.2017.2750907.
- 35 **F. Conti**, A. Marongiu, C. Pilkington, and L. Benini, "He-p2012: Performance and energy exploration of architecturally heterogeneous many-cores," *J. Signal Process. Syst.*, vol. 85, no. 3, pp. 325–340, 2016.  DOI: 10.1007/S11265-015-1056-7.
- 36 **F. Conti**, D. Rossi, A. Pullini, I. Loi, and L. Benini, "PULP: A ultra-low power parallel accelerator for energy-efficient and flexible embedded vision," *J. Signal Process. Syst.*, vol. 84, no. 3, pp. 339–354, 2016.  DOI: 10.1007/S11265-015-1070-9.
- 37 G. Tuveri, P. Meloni, F. Palumbo, G. P. Seu, I. Loi, **F. Conti**, and L. Raffo, "On-the-fly adaptivity for process networks over shared-memory platforms," *Microprocess. Microsystems*, vol. 46, pp. 240–254, 2016.  DOI: 10.1016/J.MICPRO.2016.06.010.

Conference Proceedings

- 1 L. Bompani, M. Rusci, D. Palossi, **F. Conti**, and L. Benini, "Multi-resolution rescored bytetrack for video object detection on ultra-low-power embedded systems," in *Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition*, 2024, pp. 2182–2190.
- 2 A. Dequino, A. Carpegna, D. Nadalini, A. Savino, L. Benini, S. Di Carlo, and **F. Conti**, "Compressed latent replays for lightweight continual learning on spiking neural networks," in *IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2024, Knoxville, Tennessee, USA, July 1-3, 2024*, IEEE, 2024, pp. 1–6.
- 3 F. Paissan, D. Nadalini, M. Rusci, A. Ancilotto, **F. Conti**, L. Benini, and E. Farella, "Structured sparse back-propagation for lightweight on-device continual learning on microcontroller units," in *Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR) Workshops*, Jun. 2024, pp. 2172–2181.
- 4 N. Bruschi, G. Tagliavini, A. Garofalo, **F. Conti**, I. Boybat, L. Benini, and D. Rossi, "End-to-end DNN inference on a massively parallel analog in memory computing architecture," in *Design, Automation & Test in Europe Conference & Exhibition, DATE 2023, Antwerp, Belgium, April 17-19, 2023*, IEEE, 2023, pp. 1–6.  DOI: 10.23919/DATE56975.2023.10137208.
- 5 **F. Conti**, D. Rossi, G. Paulin, A. Garofalo, A. D. Mauro, G. Rutishauser, G. Ottavi, M. Eggimann, H. Okuhara, V. Huard, O. Montfort, L. Jure, N. Exhibard, P. Gouedo, M. Louvat, E. Botte, and L. Benini, "A 12.4tops/w @ 136gops ai-iot system-on-chip with 16 risc-v, 2-to-8b precision-scalable DNN acceleration and 30%-boost adaptive body biasing," in *IEEE International Solid-State Circuits Conference, ISSCC 2023, San Francisco, CA, USA, February 19-23, 2023*, IEEE, 2023, pp. 326–327.  DOI: 10.1109/ISSCC42615.2023.10067643.
- 6 J. V. Delm, M. Vandersteegen, A. Burrello, G. M. Sarda, **F. Conti**, D. J. Pagliari, L. Benini, and M. Verhelst, "HTVM: efficient neural network deployment on heterogeneous tinymml platforms," in *60th ACM/IEEE Design Automation Conference, DAC 2023, San Francisco, CA, USA, July 9-13, 2023*, IEEE, 2023, pp. 1–6.  DOI: 10.1109/DAC56929.2023.10247664.
- 7 W. Fornaciari, F. Reghenzani, G. Agosta, D. Zoni, A. Galimberti, **F. Conti**, Y. Tortorella, E. Parisi, F. Barchi, A. Bartolini, A. Acquaviva, D. Gregori, S. Cognetta, C. Ciancarelli, A. Leboffe, P. Serri, A. Burrello, D. J. Pagliari, G. Urgese, M. Martina, G. Masera, R. D. Carlo, and A. Sciarappa, "RISC-V processor technologies for aerospace applications in the ISOLDE project," in *Embedded Computer Systems: Architectures, Modeling, and Simulation - 23rd International Conference, SAMOS 2023, Samos*,

Greece, July 2-6, 2023, *Proceedings*, C. Silvano, C. Pilato, and M. Reichenbach, Eds., ser. Lecture Notes in Computer Science, vol. 14385, Springer, 2023, pp. 363-378.  DOI: 10.1007/978-3-031-46077-7_24.

- 8 L. Macan, A. Burrello, L. Benini, and **F. Conti**, “WIP: automatic DNN deployment on heterogeneous platforms: The GAP9 case study,” in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, CASES 2023, Hamburg, Germany, September 17-22, 2023*, J. Doppa and S. Bhunia, Eds., ACM/IEEE, 2023, pp. 9-10.  DOI: 10.1145/3607889.3609092.
- 9 A. Nadalini, G. Rutishauser, A. Burrello, N. Bruschi, A. Garofalo, L. Benini, **F. Conti**, and D. Rossi, “A 3 TOPS/W RISC-V parallel cluster for inference of fine-grain mixed-precision quantized neural networks,” in *IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2023, Foz do Iguacu, Brazil, June 20-23, 2023*, IEEE, 2023, pp. 1-6.  DOI: 10.1109/ISVLSI59464.2023.10238679.
- 10 A. S. Prasad, L. Benini, and **F. Conti**, “Specialization meets flexibility: A heterogeneous architecture for high-efficiency, high-flexibility AR/VR processing,” in *60th ACM/IEEE Design Automation Conference, DAC 2023, San Francisco, CA, USA, July 9-13, 2023*, IEEE, 2023, pp. 1-6.  DOI: 10.1109/DAC56929.2023.10247945.
- 11 G. Rutishauser, **F. Conti**, and L. Benini, “Free bits: Latency optimization of mixed-precision quantized neural networks on the edge,” in *5th IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2023, Hangzhou, China, June 11-13, 2023*, IEEE, 2023, pp. 1-5.  DOI: 10.1109/AICAS57966.2023.10168577.
- 12 M. Scherer, M. Eggimann, A. D. Mauro, A. S. Prasad, **F. Conti**, D. Rossi, J. T. Gómez, Z. Li, S. S. Sarwar, Z. Wang, B. D. Salvo, and L. Benini, “Siracusa: A low-power on-sensor RISC-V soc for extended reality visual processing in 16nm CMOS,” in *49th IEEE European Solid State Circuits Conference, ESSCIRC 2023, Lisbon, Portugal, September 11-14, 2023*, IEEE, 2023, pp. 217-220.  DOI: 10.1109/ESSCIRC59616.2023.10268718.
- 13 M. Sinigaglia, L. Bertaccini, L. Valente, A. Garofalo, S. Benatti, L. Benini, **F. Conti**, and D. Rossi, “ECHOES: a 200 GOPS/W frequency domain soc with FFT processor and i²s DSP for flexible data acquisition from microphone arrays,” in *IEEE International Symposium on Circuits and Systems, ISCAS 2023, Monterey, CA, USA, May 21-25, 2023*, IEEE, 2023, pp. 1-5.  DOI: 10.1109/ISCAS46773.2023.10181862.
- 14 M. Ulbricht, Y. Tortorella, M. Rogenmoser, L. Lu, J. Chen, **F. Conti**, M. Krstic, and L. Benini, “PULP fiction no more - dependable PULP systems for space,” in *IEEE European Test Symposium, ETS 2023, Venezia, Italy, May 22-26, 2023*, IEEE, 2023, pp. 1-10.  DOI: 10.1109/ETS56758.2023.10174164.
- 15 N. Bruschi, G. Tagliavini, **F. Conti**, S. Abadal, A. Cabellos-Aparicio, E. Alarcón, G. Karunaratne, I. Boybat, L. Benini, and D. Rossi, “Scale up your in-memory accelerator: Leveraging wireless-on-chip communication for aimc-based CNN inference,” in *4th IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2022, Incheon, Republic of Korea, June 13-15, 2022*, IEEE, 2022, pp. 170-173.  DOI: 10.1109/AICAS54282.2022.9869996.
- 16 A. Dequino, **F. Conti**, and L. Benini, “Vit-lr: Pushing the envelope for transformer-based on-device embedded continual learning,” in *13th IEEE International Green and Sustainable Computing Conference, IGSC 2022, Pittsburgh, PA, USA, October 24-25, 2022*, IEEE, 2022, pp. 1-6.  DOI: 10.1109/IGSC55832.2022.9969361.
- 17 A. Garofalo, M. Perotti, L. Valente, Y. Tortorella, A. Nadalini, L. Benini, D. Rossi, and **F. Conti**, “Darkside: 2.6gflops, 8.7mw heterogeneous RISC-V cluster for extreme-edge on-chip DNN inference and training,” in *48th IEEE European Solid State Circuits Conference, ESSCIRC 2022, Milan, Italy, September 19-22, 2022*, IEEE, 2022, pp. 273-276.  DOI: 10.1109/ESSCIRC55480.2022.9911384.
- 18 A. D. Mauro, A. S. Prasad, Z. Huang, M. Spallanzani, **F. Conti**, and L. Benini, “SNE: an energy-proportional digital accelerator for sparse event-based convolutions,” in *2022 Design, Automation & Test in Europe Conference & Exhibition, DATE 2022, Antwerp, Belgium, March 14-23, 2022*,

C. Bolchini, I. Verbauwhede, and I. Vatajelu, Eds., IEEE, 2022, pp. 825–830.  DOI: 10.23919/DATE54114.2022.9774552.

- 19 D. Nadalini, M. Rusci, G. Tagliavini, L. Ravaglia, L. Benini, and **F. Conti**, “Pulp-trainlib: Enabling on-device training for RISC-V multi-core mcus through performance-driven autotuning,” in *Embedded Computer Systems: Architectures, Modeling, and Simulation - 22nd International Conference, SAMOS 2022, Samos, Greece, July 3-7, 2022, Proceedings*, A. Orailoglu, M. Reichenbach, and M. Jung, Eds., ser. Lecture Notes in Computer Science, vol. 13511, Springer, 2022, pp. 200–216.  DOI: 10.1007/978-3-031-15074-6_13.
- 20 M. Orlandi, M. Zanghieri, V. J. K. Morinigo, **F. Conti**, P. D. Schiavone, L. Benini, and S. Benatti, “Semg neural spikes reconstruction for gesture recognition on a low-power multicore processor,” in *IEEE Biomedical Circuits and Systems Conference, BioCAS 2022, Taipei, Taiwan, October 13-15, 2022*, IEEE, 2022, pp. 704–708.  DOI: 10.1109/BIOCAS54905.2022.9948617.
- 21 M. Orlandi, M. Zanghieri, P. D. Schiavone, E. Donati, **F. Conti**, and S. Benatti, “Motor-unit ordering of blindly-separated surface-emg signals for gesture recognition,” in *Advances in System-Integrated Intelligence - Proceedings of the 6th International Conference on System-Integrated Intelligence (SysInt 2022), September 7-9, 2022, Genova, Italy*, M. Valle, D. Lehmhus, C. Gianoglio, E. Ragusa, L. Seminara, S. Bosse, A. Ibrahim, and K. Thoben, Eds., ser. Lecture Notes in Networks and Systems, vol. 546, Springer, 2022, pp. 518–529.  DOI: 10.1007/978-3-031-16281-7_49.
- 22 Y. Tortorella, L. Bertaccini, D. Rossi, L. Benini, and **F. Conti**, “Redmule: A compact FP16 matrix-multiplication accelerator for adaptive deep learning on risc-v-based ultra-low-power socs,” in *2022 Design, Automation & Test in Europe Conference & Exhibition, DATE 2022, Antwerp, Belgium, March 14-23, 2022*, C. Bolchini, I. Verbauwhede, and I. Vatajelu, Eds., IEEE, 2022, pp. 1099–1102.  DOI: 10.23919/DATE54114.2022.9774759.
- 23 G. Bellocchi, A. Capotondi, **F. Conti**, and A. Marongiu, “A risc-v-based FPGA overlay to simplify embedded accelerator deployment,” in *24th Euromicro Conference on Digital System Design, DSD 2021, Virtual Event / Palermo, Sicily, Italy, September 1-3, 2021*, F. Leporati, S. Vitabile, and A. Skavhaug, Eds., IEEE, 2021, pp. 9–17.  DOI: 10.1109/DSD53832.2021.00011.
- 24 L. Bertaccini, L. Benini, and **F. Conti**, “To buffer, or not to buffer? A case study on FFT accelerators for ultra-low-power multicore clusters,” in *32nd IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP 2021, Virtual Conference, USA, July 7-9, 2021*, IEEE, 2021, pp. 1–8.  DOI: 10.1109/ASAP52443.2021.00008.
- 25 N. Bruschi, G. Haugou, G. Tagliavini, **F. Conti**, L. Benini, and D. Rossi, “Gvsoc: A highly configurable, fast and accurate full-platform simulator for RISC-V based iot processors,” in *39th IEEE International Conference on Computer Design, ICCD 2021, Storrs, CT, USA, October 24-27, 2021*, IEEE, 2021, pp. 409–416.  DOI: 10.1109/ICCD53106.2021.00071.
- 26 A. Burrello, A. Dequino, D. J. Pagliari, **F. Conti**, M. Zanghieri, E. Macii, L. Benini, and M. Poncino, “TCN mapping optimization for ultra-low power time-series edge inference,” in *IEEE/ACM International Symposium on Low Power Electronics and Design, ISLPED 2021, Boston, MA, USA, July 26-28, 2021*, IEEE, 2021, pp. 1–6.  DOI: 10.1109/ISLPED52811.2021.9502494.
- 27 A. Burrello, M. Scherer, M. Zanghieri, **F. Conti**, and L. Benini, “A microcontroller is all you need: Enabling transformer execution on low-power iot endnodes,” in *2021 IEEE International Conference on Omni-Layer Intelligent Systems, COINS 2021, Barcelona, Spain, August 23-25, 2021*, IEEE, 2021, pp. 1–6.  DOI: 10.1109/COINS51742.2021.9524173.
- 28 M. Capra, **F. Conti**, and M. Martina, “A multi-precision bit-serial hardware accelerator IP for deep learning enabled internet-of-things,” in *64th IEEE International Midwest Symposium on Circuits and Systems, MWSCAS 2021, Lansing, MI, USA, August 9-11, 2021*, IEEE, 2021, pp. 192–197.  DOI: 10.1109/MWSCAS47672.2021.9531722.

- 29 A. Garofalo, G. Ottavi, A. D. Mauro, **F. Conti**, G. Tagliavini, L. Benini, and D. Rossi, "A 1.15 tops/w, 16-cores parallel ultra-low power cluster with 2b-to-32b fully flexible bit-precision and vector lockstep execution mode," in *47th ESSCIRC 2021 - European Solid State Circuits Conference, ESSCIR 2021, Grenoble, France, September 13-22, 2021*, IEEE, 2021, pp. 267–270.  DOI: 10.1109/ESSCIRC53450.2021.9567767.
- 30 A. Garofalo, G. Tagliavini, **F. Conti**, L. Benini, and D. Rossi, "Xpulpnn: Enabling energy efficient and flexible inference of quantized neural networks on RISC-V based iot end nodes," in *28th IEEE Symposium on Computer Arithmetic, ARITH 2021, Lyngby, Denmark, June 14-16, 2021*, IEEE, 2021, p. 53.  DOI: 10.1109/ARITH51176.2021.00020.
- 31 J. Klein, A. Levisse, G. Ansaloni, D. Atienza, M. Zapater, M. Dazzi, G. Karunaratne, I. Boybat, A. Sebastian, D. Rossi, **F. Conti**, E. P. de Santana, P. H. Bolívar, M. Saeed, R. Negra, Z. Wang, K. Wang, M. C. Lemme, A. Jain, R. Guirado, H. Taghvaei, and S. Abadal, "Architecting more than moore: Wireless plasticity for massive heterogeneous computer architectures (wiplash)," in *CF '21: Computing Frontiers Conference, Virtual Event, Italy, May 11-13, 2021*, M. Palesi, A. Tumeo, G. I. Goumas, and C. G. Almudéver, Eds., ACM, 2021, pp. 191–193.  DOI: 10.1145/3457388.3458859.
- 32 H. Müller, D. Palossi, S. Mach, **F. Conti**, and L. Benini, "Fünfiber-drone: A modular open-platform 18-grams autonomous nano-drone," in *Design, Automation & Test in Europe Conference & Exhibition, DATE 2021, Grenoble, France, February 1-5, 2021*, IEEE, 2021, pp. 1610–1615.  DOI: 10.23919/DATE51398.2021.9474262.
- 33 G. Ottavi, G. Karunaratne, **F. Conti**, I. Boybat, L. Benini, and D. Rossi, "End-to-end 100-tops/w inference with analog in-memory computing: Are we there yet?" In *3rd IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2021, Washington, DC, USA, June 6-9, 2021*, IEEE, 2021, pp. 1–4.  DOI: 10.1109/AICAS51828.2021.9458409.
- 34 M. Risso, A. Burrello, D. J. Pagliari, **F. Conti**, L. Lamberti, E. Macii, L. Benini, and M. Poncino, "Pruning in time (PIT): A lightweight network architecture optimizer for temporal convolutional networks," in *58th ACM/IEEE Design Automation Conference, DAC 2021, San Francisco, CA, USA, December 5-9, 2021*, IEEE, 2021, pp. 1015–1020.  DOI: 10.1109/DAC18074.2021.9586187.
- 35 D. Rossi, **F. Conti**, M. Eggimann, S. Mach, A. D. Mauro, M. Guermendi, G. Tagliavini, A. Pullini, I. Loi, J. Chen, E. Flamand, and L. Benini, "4.4 A 1.3tops/w @ 32gops fully integrated 10-core soc for iot end-nodes with 1.7 μ W cognitive wake-up from mram-based state-retentive sleep mode," in *IEEE International Solid-State Circuits Conference, ISSCC 2021, San Francisco, CA, USA, February 13-22, 2021*, IEEE, 2021, pp. 60–62.  DOI: 10.1109/ISSCC42613.2021.9365939.
- 36 N. Bruschi, A. Garofalo, **F. Conti**, G. Tagliavini, and D. Rossi, "Enabling mixed-precision quantized neural networks in extreme-edge devices," in *Proceedings of the 17th ACM International Conference on Computing Frontiers, CF 2020, Catania, Sicily, Italy, May 11-13, 2020*, M. Palesi, G. Palermo, C. Graves, and E. Arima, Eds., ACM, 2020, pp. 217–220.  DOI: 10.1145/3387902.3394038.
- 37 A. Garofalo, G. Tagliavini, **F. Conti**, D. Rossi, and L. Benini, "Xpulpnn: Accelerating quantized neural networks on RISC-V processors through ISA extensions," in *2020 Design, Automation & Test in Europe Conference & Exhibition, DATE 2020, Grenoble, France, March 9-13, 2020*, IEEE, 2020, pp. 186–191.  DOI: 10.23919/DATE48585.2020.9116529.
- 38 G. Ottavi, A. Garofalo, G. Tagliavini, **F. Conti**, L. Benini, and D. Rossi, "A mixed-precision RISC-V processor for extreme-edge DNN inference," in *2020 IEEE Computer Society Annual Symposium on VLSI, ISVLSI 2020, Limassol, Cyprus, July 6-8, 2020*, IEEE, 2020, pp. 512–517.  DOI: 10.1109/ISVLSI49217.2020.000-5.
- 39 L. Ravaglia, M. Rusci, A. Capotondi, **F. Conti**, L. Pellegrini, V. Lomonaco, D. Maltoni, and L. Benini, "Memory-latency-accuracy trade-offs for continual learning on a RISC-V extreme-edge node," in *IEEE Workshop on Signal Processing Systems, SiPS 2020, Coimbra, Portugal, October 20-22, 2020*, IEEE, 2020, pp. 1–6.  DOI: 10.1109/SIPS0750.2020.9195220.

- 40 M. Zanghieri, S. Benatti, **F. Conti**, A. Burrello, and L. Benini, "Temporal variability analysis in semg hand grasp recognition using temporal convolutional networks," in *2nd IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2020, Genova, Italy, August 31 - September 2, 2020*, IEEE, 2020, pp. 228–232.  DOI: 10.1109/AICAS48895.2020.9073888.
- 41 A. Burrello, **F. Conti**, A. Garofalo, D. Rossi, and L. Benini, "DORY: lightweight memory hierarchy management for deep NN inference on iot endnodes: Work-in-progress," in *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis Companion, CODES+ISSS 2019, part of ESWEEK 2019, New York, NY, USA, October 13-18, 2019*, ACM, 2019, 17:1–17:2.  DOI: 10.1145/3349567.3351726.
- 42 A. Garofalo, M. Rusci, **F. Conti**, D. Rossi, and L. Benini, "PULP-NN: A computing library for quantized neural network inference at the edge on RISC-V based parallel ultra low power clusters," in *26th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2019, Genoa, Italy, November 27-29, 2019*, IEEE, 2019, pp. 33–36.  DOI: 10.1109/ICECS46596.2019.8965067.
- 43 P. Meloni, D. Loi, P. Busia, G. Deriu, A. D. Pimentel, D. Sapra, T. P. Stefanov, S. Minakova, **F. Conti**, L. Benini, M. Pintor, B. Biggio, B. Moser, N. Shepeleva, N. Fragoulis, I. Theodorakopoulos, M. Masin, and F. Palumbo, "Optimization and deployment of cnns at the edge: The ALOHA experience," in *Proceedings of the 16th ACM International Conference on Computing Frontiers, CF 2019, Alghero, Italy, April 30 - May 2, 2019*, F. Palumbo, M. Becchi, M. Schulz, and K. Sato, Eds., ACM, 2019, pp. 326–332.  DOI: 10.1145/3310273.3323435.
- 44 D. Palossi, **F. Conti**, and L. Benini, "An open source and open hardware deep learning-powered visual navigation engine for autonomous nano-uavs," in *15th International Conference on Distributed Computing in Sensor Systems, DCOSS 2019, Santorini, Greece, May 29-31, 2019*, IEEE, 2019, pp. 604–611.  DOI: 10.1109/DCOSS.2019.00111.
- 45 **F. Conti**, L. Cavigelli, G. Paulin, I. Susmelj, and L. Benini, "Chipmunk: A systolically scalable 0.9 mm², 3.08gop/s/mw @ 1.2 mw accelerator for near-sensor recurrent neural network inference," in *2018 IEEE Custom Integrated Circuits Conference, CICC 2018, San Diego, CA, USA, April 8-11, 2018*, IEEE, 2018, pp. 1–4.  DOI: 10.1109/CICC.2018.8357068.
- 46 E. Flamand, D. Rossi, **F. Conti**, I. Loi, A. Pullini, F. Rotenberg, and L. Benini, "GAP-8: A RISC-V soc for AI at the edge of the iot," in *29th IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP 2018, Milano, Italy, July 10-12, 2018*, IEEE Computer Society, 2018, pp. 1–4.  DOI: 10.1109/ASAP.2018.8445101.
- 47 A. Gomez, **F. Conti**, and L. Benini, "Thermal image-based cnn's for ultra-low power people recognition," in *Proceedings of the 15th ACM International Conference on Computing Frontiers, CF 2018, Ischia, Italy, May 08-10, 2018*, D. R. Kaeli and M. Pericàs, Eds., ACM, 2018, pp. 326–331.  DOI: 10.1145/3203217.3204465.
- 48 P. Meloni, D. Loi, G. Deriu, A. D. Pimentel, D. Sapra, B. Moser, N. Shepeleva, **F. Conti**, L. Benini, O. Ripolles, D. Solans, M. Pintor, B. Biggio, T. P. Stefanov, S. Minakova, N. Fragoulis, I. Theodorakopoulos, M. Masin, and F. Palumbo, "ALOHA: an architectural-aware framework for deep learning at the edge," in *Proceedings of the Workshop on INTElligent Embedded Systems Architectures and Applications, INTESA@ESWEEK 2018, Turin, Italy, October 04-04, 2018*, M. Martina and W. Fornaciari, Eds., ACM, 2018, pp. 19–26.  DOI: 10.1145/3285017.3285019.
- 49 P. Meloni, D. Loi, G. Deriu, A. D. Pimentel, D. Sapra, M. Pintor, B. Biggio, O. Ripolles, D. Solans, **F. Conti**, L. Benini, T. P. Stefanov, S. Minakova, B. Moser, N. Shepeleva, M. Masin, F. Palumbo, N. Fragoulis, and I. Theodorakopoulos, "Architecture-aware design and implementation of CNN algorithms for embedded inference: The ALOHA project," in *30th International Conference on Microelectronics, ICM 2018, Sousse, Tunisia, December 16-19, 2018*, IEEE, 2018, pp. 52–55.  DOI: 10.1109/ICM.2018.8704093.

- 50 M. Rusci, A. Capotondi, **F. Conti**, and L. Benini, "Quantized nns as the definitive solution for inference on low-power ARM mcus?: Work-in-progress," in *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2018, part of ESWEK 2018, Torino, Italy, September 30 - October 5, 2018*, A. Shrivastava and S. Pasricha, Eds., IEEE / ACM, 2018, p. 12.  DOI: 10.1109/CODESISSS.2018.8525915.
- 51 F. K. Gürkaynak, R. Schilling, M. Muehlberghuber, **F. Conti**, S. Mangard, and L. Benini, "Multi-core data analytics soc with a flexible 1.76 gbit/s AES-XTS cryptographic accelerator in 65 nm CMOS," in *Proceedings of the Fourth Workshop on Cryptography and Security in Computing Systems, CS2@HiPEAC 2017, Stockholm, Sweden, January 24, 2017*, M. Brorsson, Z. Lu, G. Agosta, A. Barenghi, and G. Pelosi, Eds., ACM, 2017, pp. 19–24.  DOI: 10.1145/3031836.3031840.
- 52 A. D. Mauro, **F. Conti**, and L. Benini, "An ultra-low power address-event sensor interface for energy-proportional time-to-information extraction," in *Proceedings of the 54th Annual Design Automation Conference, DAC 2017, Austin, TX, USA, June 18-22, 2017*, ACM, 2017, 75:1–75:6.  DOI: 10.1145/3061639.3062201.
- 53 P. D. Schiavone, **F. Conti**, D. Rossi, M. Gautschi, A. Pullini, E. Flamand, and L. Benini, "Slow and steady wins the race? A comparison of ultra-low-power RISC-V cores for internet-of-things applications," in *27th International Symposium on Power and Timing Modeling, Optimization and Simulation, PATMOS 2017, Thessaloniki, Greece, September 25-27, 2017*, IEEE, 2017, pp. 1–8.  DOI: 10.1109/PATMOS.2017.8106976.
- 54 **F. Conti**, D. Palossi, A. Marongiu, D. Rossi, and L. Benini, "Enabling the heterogeneous accelerator model on ultra-low power microcontroller platforms," in *2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016, Dresden, Germany, March 14-18, 2016*, L. Fanucci and J. Teich, Eds., IEEE, 2016, pp. 1201–1206.  URL: <https://ieeexplore.ieee.org/document/7459494/>.
- 55 P. Meloni, G. Deriu, **F. Conti**, I. Loi, L. Raffo, and L. Benini, "A high-efficiency runtime reconfigurable IP for CNN acceleration on a mid-range all-programmable soc," in *International Conference on ReConFigurable Computing and FPGAs, ReConFig 2016, Cancun, Mexico, November 30 - Dec. 2, 2016*, P. M. Athanas, R. Cumplido, C. Feregrino, and R. Sass, Eds., IEEE, 2016, pp. 1–8.  DOI: 10.1109/RECONFIG.2016.7857144.
- 56 P. Meloni, G. Deriu, **F. Conti**, I. Loi, L. Raffo, and L. Benini, "Curbing the roofline: A scalable and flexible architecture for cnns on FPGA," in *Proceedings of the ACM International Conference on Computing Frontiers, CF'16, Como, Italy, May 16-19, 2016*, G. Palermo and J. Feo, Eds., ACM, 2016, pp. 376–383.  DOI: 10.1145/2903150.2911715.
- 57 A. Pullini, **F. Conti**, D. Rossi, I. Loi, M. Gautschi, and L. Benini, "A heterogeneous multi-core system-on-chip for energy efficient brain inspired vision," in *IEEE International Symposium on Circuits and Systems, ISCAS 2016, Montréal, QC, Canada, May 22-25, 2016*, IEEE, 2016, p. 2910.  DOI: 10.1109/ISCAS.2016.7539213.
- 58 **F. Conti** and L. Benini, "A ultra-low-energy convolution engine for fast brain-inspired vision in multicore clusters," in *Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition, DATE 2015, Grenoble, France, March 9-13, 2015*, W. Nebel and D. Atienza, Eds., ACM, 2015, pp. 683–688.  URL: <http://dl.acm.org/citation.cfm?id=2755910>.
- 59 D. Rossi, **F. Conti**, A. Marongiu, A. Pullini, I. Loi, M. Gautschi, G. Tagliavini, A. Capotondi, P. Flatresse, and L. Benini, "PULP: A parallel ultra low power platform for next generation iot applications," in *2015 IEEE Hot Chips 27 Symposium (HCS), Cupertino, CA, USA, August 22-25, 2015*, IEEE, 2015, pp. 1–39.  DOI: 10.1109/HOTCHIPS.2015.7477325.
- 60 P. Burgio, G. Tagliavini, **F. Conti**, A. Marongiu, and L. Benini, "Tightly-coupled hardware support to dynamic parallelism acceleration in embedded shared memory clusters," in *Design, Automation & Test in Europe Conference & Exhibition, DATE 2014, Dresden, Germany, March 24-28, 2014*, G. P. Fettweis and

W. Nebel, Eds., European Design and Automation Association, 2014, pp. 1–6.  DOI: 10.7873/DATE.2014.169.

- 61 **F. Conti**, C. Pilkington, A. Marongiu, and L. Benini, “He-p2012: Architectural heterogeneity exploration on a scalable many-core platform,” in *IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2014, Zurich, Switzerland, June 18–20, 2014*, IEEE Computer Society, 2014, pp. 114–120.  DOI: 10.1109/ASAP.2014.6868645.
- 62 **F. Conti**, C. Pilkington, A. Marongiu, and L. Benini, “He-p2012: Architectural heterogeneity exploration on a scalable many-core platform,” in *Great Lakes Symposium on VLSI 2014, GLSVLSI '14, Houston, TX, USA - May 21 - 23, 2014*, J. R. Cavallaro, T. Zhang, A. K. Jones, and H. (Li, Eds., ACM, 2014, pp. 231–232.  DOI: 10.1145/2591513.2591553.
- 63 **F. Conti**, A. Pullini, and L. Benini, “Brain-inspired classroom occupancy monitoring on a low-power mobile platform,” in *IEEE Conference on Computer Vision and Pattern Recognition, CVPR Workshops 2014, Columbus, OH, USA, June 23–28, 2014*, IEEE Computer Society, 2014, pp. 624–629.  DOI: 10.1109/CVPRW.2014.95.
- 64 **F. Conti**, D. Rossi, A. Pullini, I. Loi, and L. Benini, “Energy-efficient vision on the PULP platform for ultra-low power parallel computing,” in *2014 IEEE Workshop on Signal Processing Systems, SiPS 2014, Belfast, United Kingdom, October 20–22, 2014*, IEEE, 2014, pp. 274–279.  DOI: 10.1109/SIPS.2014.6986099.
- 65 P. Meloni, G. Tuveri, L. Raffo, I. Loi, and **F. Conti**, “A stream buffer mechanism for pervasive splitting transformations on polyhedral process networks,” in *Proceedings of the 2nd International Workshop on Many-core Embedded Systems, MES'2014, in conjunction with the 41st International Symposium on Computer Architecture, ISCA'2014, Minneapolis, MN, USA, June 15, 2014*, M. Daneshtalab, M. Ebrahimi, M. Palesi, F. Angiolini, and J. Plosila, Eds., ACM, 2014, pp. 25–32.  DOI: 10.1145/2613908.2613913.
- 66 P. Meloni, G. Tuveri, L. Raffo, I. Loi, and **F. Conti**, “Online process transformation for polyhedral process networks in shared-memory mpsoCs,” in *3rd Mediterranean Conference on Embedded Computing, MECO 2014, Budva, Montenegro, June 15–19, 2014*, IEEE, 2014, pp. 92–97.  DOI: 10.1109/MECO.2014.6862666.
- 67 **F. Conti**, A. Marongiu, and L. Benini, “Synthesis-friendly techniques for tightly-coupled integration of hardware accelerators into shared-memory multi-core clusters,” in *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2013, Montreal, QC, Canada, September 29 - October 4, 2013*, IEEE, 2013, 5:1–5:10.  DOI: 10.1109/CODES- ISSS.2013.6658992.

Books and Chapters

- 1 **F. Conti**, F. Indirli, A. Latella, F. Papariello, G. M. Puglia, F. Tecce, G. Urlini, and M. Zanghieri, “Ai-powered collision avoidance safety system for industrial woodworking machinery,” in *Artificial Intelligence for Digitising Industry–Applications*, River Publishers, 2022, pp. 187–204.
- 2 **F. Conti**, M. Rusci, and L. Benini, “The memory challenge in ultra-low power deep learning,” in *NANO-CHIPS 2030: On-Chip AI for an Efficient Data-Driven World*, B. Murmann and B. Hoefflinger, Eds., Cham: Springer International Publishing, 2020, pp. 323–349, ISBN: 978-3-030-18338-7.  DOI: 10.1007/978-3-030-18338-7_19.

Skills

Languages	 Italian (mothertongue), English (listening: C1, reading: C2, spoken production: C1, spoken interaction: C1, writing: C2).
Coding	 SystemVerilog , C, C++, Bash, Python (+ PyTorch), Rust, ...
Misc.	 Academic research, teaching, training, consultation, $\text{\LaTeX}$ typesetting and publishing.